Digital Channelizing Radio Frequency Receiver

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***Abstract*—HYPRES is developing a class of digital receivers featuring direct digitization at radio frequency (RF). Such a receiver consists of a wideband analog-to-digital converter (ADC) modulator and multiple digital channelizer units to extract different frequency bands-of-interest within the broad digitized spectrum. The single-bit oversampled data, from either a lowpass delta or bandpass delta-sigma modulator, are applied to one or more channelizers, each comprising digital in-phase and quadrature mixers and a pair of digital decimation filters. We perform channelization in two steps, the first at full ADC sampling clock frequency with rapid single flux quantum (RSFQ) digital circuits and the second at reduced (decimated) clock frequency with commercial field programmable gate array (FPGA) chips at room temperature. We have demonstrated lowpass and bandpass digital receivers by integrating an ADC modulator and a channelizer unit on the same chip at clock frequencies up to 20 GHz. These 1-cm^2 single-chip digital-RF receivers contain over 10,000 Josephson junctions. The channelizing receiver approach can be extended to include multiple ADC modulators and multiple channelizer units on a multi-chip module.**

***Index Terms*—ADC, digital filter, digital-RF, niobium, RSFQ, software radio, superconductor.**

I. Introduction

ONE of the most promising applications for superconductor electronics is in the area of RF communications. Future military and commercial radio frequency (RF) systems demand better utilization of the RF spectrum, moving towards higher frequency, wider bandwidth, and greater flexibility to accommodate diverse modalities (e.g. voice, data, video, detection and ranging, electronic countermeasures). The conventional analog RF technology not only fails to meet but also fails to show a credible development path for meeting these demands in the future. Extension of digital processing to the traditionally analog RF domain, also known as the *software radio* concept [1], provides a path to circumvent the limitations of traditional single-band, single-mode radios that have limited or no networking capability. The idea is to perform direct conversion of broadband RF signals to digital, facilitating software controlled digital data processing. Thus all frequency- and protocol-specific analog hardware is replaced with software-programmable digital hardware. The emergence of this software radio architecture presents an opportunity for rapid single flux quantum (RSFQ) mixed-signal technology that enables direct conversion between analog and digital domains at multi-GHz radio frequencies [2].

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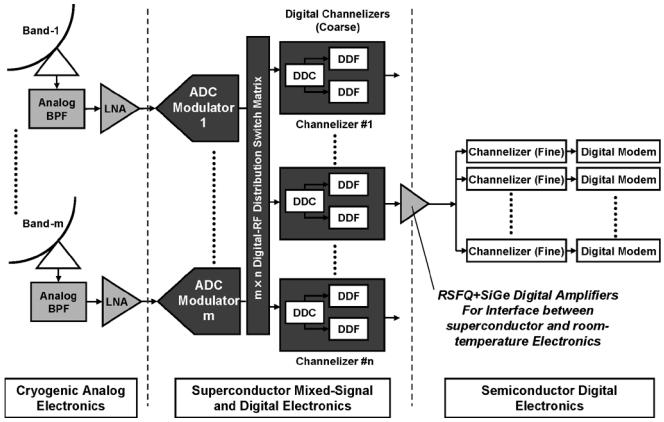

Fig. 1. Multi-band, multi-channel digital-RF channelizing receiver architecture. Each digital (coarse) channelizing unit comprises a digital downconverter (DDC) and two digital decimation filters (DDF).

II. Digital-RF Channelizing Receiver

HYPRES has developed a multi-band, multi-channel digital-RF transceiver architecture [3]. Fig. 1 shows the essential parts of the receive side of this hybrid temperature hybrid technology (HTHT) architecture, combining different analog, mixed-signal, and digital components at various temperatures for optimum performance. We envision hosting such a digital-RF receiver on a multi-stage cryocooler. Wideband RF signals from each antenna are directly digitized at RF, and routed through a switch matrix to one or more channelizing units that can be dynamically assigned for programmable extraction of narrower sub-bands. Once the RF signals are in the digital domain, multiple copies can be generated without compromising signal power and quality. Therefore, the digital-RF signal from a single ADC can be simultaneously applied to a bank of digital channelizing units, each operating independently to extract a sub-band from a wide input band.

For a multi-band system, the digitized data streams from multiple ADC front-ends are distributed to a bank of channelizers through a digital non-blocking, multi-casting switch matrix. The switch matrix, a critical element of our digital-RF transceiver architecture, provides natural partitioning between band-specific components, such as antennas, analog filters, and ADCs, and band-independent components, such as digital channelizers. This architecture is scalable to an arbitrary number of channelizers (or more general digital processors) and banded antenna-ADC pairs. Furthermore, the digital switch matrix can be programmed in real time to dynamically reconfigure the communication system: changing band-to-channel allocation, cross-banding, etc.

Digital channel extraction is performed in two steps: coarse channelization at the full ADC sample rate (currently, up to

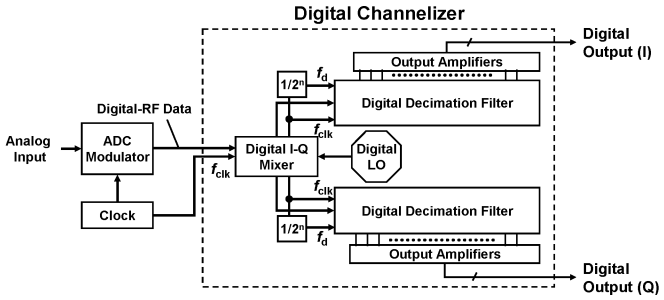

Fig. 2. Block diagram of a digital channelizer comprising a digital in-phase (I) and quadrature (Q) digital mixer and two digital decimation filters.

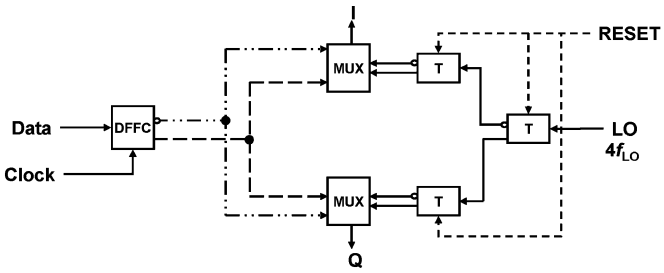

Fig. 3. Digital in-phase and quadrature single-bit mixer.

40 GHz) in superconductor electronics (SCE), and finer channelization at reduced (decimated) clock rate with commercial FPGAs. Each digital channelizer comprises a pair of digital in-phase (I) and quadrature (Q) mixers and filters.

III. Digital Channelizer

The superconductor digital channelizer (Fig. 2) interfaces with the ultrafast oversampled analog-to-digital converters [4], which typically produce single-bit oversampled data at the sampling clock rate (up to 40 GHz with HYPRES' 4.5 $\mathrm{kA/cm^2}$ fabrication process). It is designed to receive a single-bit digital-RF data stream along with the clock. The output of the channelizer is a pair of two digital samples (I and Q) at the decimated clock rate ($f_{\mathrm{d}} = f_{\mathrm{clk}}/2^{\mathrm{n}}$).

A. Digital In-Phase and Quadrature Mixer

The first step is a digital down-conversion by multiplying (mixing) the digital-RF data with a digital local oscillator (LO). In our first generation digital channelizer, we have used a single-bit periodic waveform (square wave) as the local oscillator. Consequently, the digital multiplier of two single-bit operands takes the form of a single logic gate; for bipolar signals, the multiplier is an exclusive-OR (XOR) function. To avoid timing problems originating from the different rates of the two operands, we implemented the XOR function by applying complementary data inputs, generated by a D-flip-flop with complementary outputs (DFFC), to an asynchronous multiplexer [5] (Fig. 3). To ensure exactly 90° relative phase difference, the in-phase (I) and quadrature (Q) local-oscillator (f_{LO}) signals are derived by dividing a signal of frequency $4f_{\mathrm{LO}}$ with a binary tree of toggle flip-flops (T). This circuit was

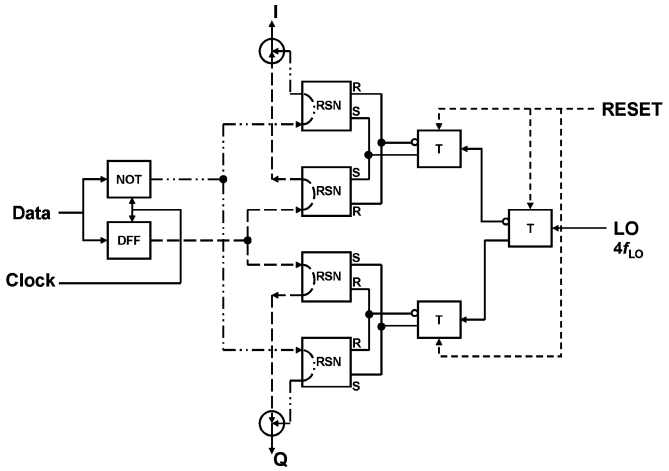

Fig. 4. Digital I and Q mixer using a pair of complementary RS flip-flops with non-destructive readout (RSN) instead of the asynchronous multiplexer.

designed for both 1 and 4.5 $\mathrm{kA/cm^2}$ fabrication processes, and demonstrated to operate with a clock frequency above 40 GHz for both.

Subsequently, we designed a more robust, but less compact, digital mixer using a pair of RS flip-flops with non-destructive readout (RSN) cells to replace each multiplexer cell (Fig. 4). The DFFC was also replaced with a D-flip-flop (DFF) and a clocked inverter (NOT) cell. This design proved to be far less susceptible to magnetic fields caused by errant ground plane currents induced by large bias currents of the nearby massive digital filters.

B. Digital Decimation Filter

The channelizer (Fig. 2) includes two second-order digital cascaded integrator comb (CIC) decimation filters (DDFs) [6]. Although these filters do not possess ideal passband characteristics and sharp cut-off, their use is quite adequate for our purposes.

First, the CIC filter does not require multipliers and is therefore the fastest. Since our ADCs are sampled at very high speed, the filter must also operate at the same high speed (20-40 GHz). In fact, most other single-bit fast delta-sigma ADCs use also CIC filters for the same reason.

Second, digital channelization is performed in two stages. The first, the fastest filter does not have to possess ideal passband and stopband characteristics as long as subsequent stages can compensate by correcting the gain droop in the passband and defining sharp high-order cut-off on the narrower bandwidth. In our case, this is emphasized by the fact that the oversampling ratio is very high. The initial CIC filter does not need to reduce the sample rate all the way down to the required Nyquist sample rate but only to a low enough rate (below 400 MHz for the current FPGA state-of-the-art) for the room-temperature electronics to perform the subsequent filtering function.

Finally, a multi-rate filter technique allows the integrator and the differentiator (comb filter) to operate at different sample rates by introducing a down-sampler (also known as a decimator

or rate changer) between them. Now even the lower-rate differentiators can be transferred to slower room-temperature electronics, leaving us to perform only multiple integration stages and the decimation function.

The second-order decimation filters used in the channelizer are based on the RSFQ implementation described in [7]. They perform the second integration, rate reduction (decimation) and the first stage of comb filtering in one step with a binary counter with destructive readout at the decimated rate. The first integrator, at full clock speed, is implemented with a binary counter with non-destructive readout. Recently, we have improved the design of the toggle flip-flop with nondestructive readout (TN) cell to widen its operating margins, and have optimized the entire DDF to comply with the evolving design rules [8]. Furthermore, the biasing scheme was altered to reduce the influence of magnetic field due to large bias currents. This is particularly important for the channelizer, which includes two decimation filters, and contains over 10,000 Josephson junctions. To keep the complexity as low as possible, the first integrator has been simplified from the original design [7]. Previously, all the TN modules included a half-adder (HA) cell for summing of two data pulses, one from the previous bit of the counter and the second from an external independent input, in a single clock period. In the current version, the HA cells were removed from all but the first two slices.

C. Output Drivers

The channelizer digital outputs are amplified to 1 mV or higher to facilitate interface with room-temperature electronics. Based on the high-speed high-voltage drivers [9], these output amplifiers were designed to maximize the frequency response while being constrained to a 200-μm width, defined by that of a decimation filter bitslice. The amplifier includes an RS-flip-flop based SFQ/DC converter, a JTL current amplifier, and a stack of SQUIDs. If all the SQUIDs in the stack, required to produce the desired output voltage into a 50 Ohm load, are driven by a single control line, the response time is too long. On the other hand, if the SQUIDs are driven in parallel to minimize the inductance of each control line, the JTL amplifier section grows in size. The optimized single-ended driver (Fig. 5) divides the SQUIDs in five stacks that are driven in parallel. The rise time of this device was measured to be 700 ps and the output amplitudes into a 50 Ohm load were 2.5 mV at 300 MHz and 1.3 mV at 1 GHz respectively for the 1 $\mathrm{kA/cm^2}$ process.

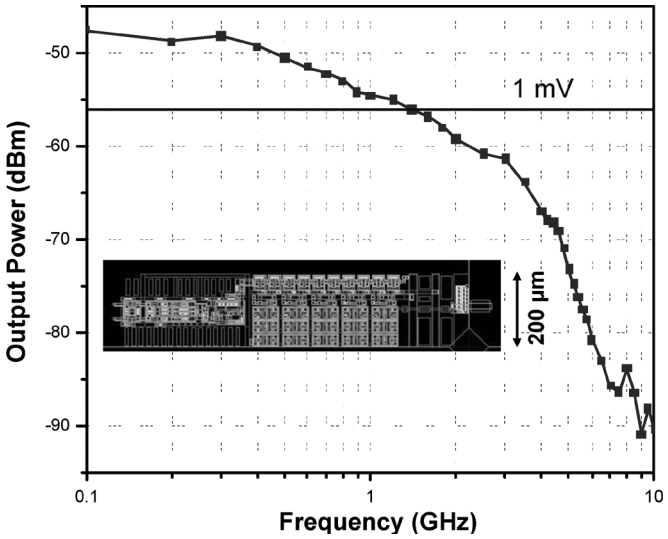

Fig. 5. Measured frequency response of the output driver with five SQUID stacks.

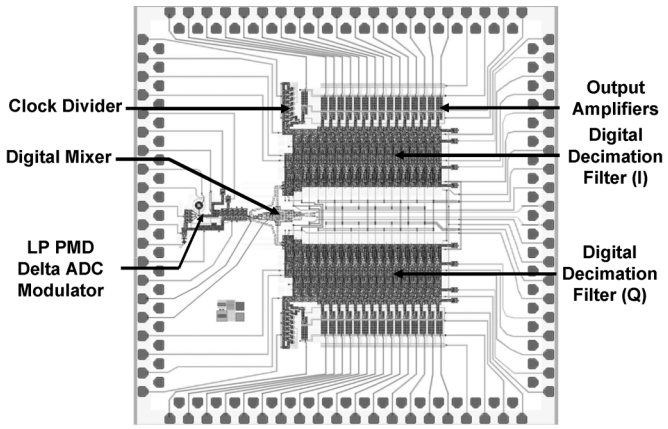

Fig. 6. Single-chip digital-RF receiver, comprising a digital channelizer attached to a lowpass phase modulation-demodulation analog-to-digital converter (LP PMD ADC).

IV. Single-Chip Digital-RF Receiver

We have designed several chips, integrating different ADCs to a digital channelizer circuit. These include a lowpass phase modulation-demodulation (LP PMD) ADC [10] and various bandpass delta-sigma ADCs [4].

A. Lowpass Digital-RF Receiver

Our very first digital receiver chip (Fig. 6) contained an LP PMD ADC modulator with a single-channel synchronizer, a digital mixer of the type shown in Fig. 3, and two 18-bitslice decimation filters, and produces 15-bit I and Q outputs at a rate of $f_{\mathrm{d}} = f_{\mathrm{clk}}/256$. Fig. 7 shows the spectra of the digital filter output for representative signals with and without local oscillator. For the standard 10 MHz signal, the measured SINAD is 74.4 dB over a bandwidth of $f_{\mathrm{d}}/2 = 39\ \mathrm{MHz}$, which compares well with 75.7 dB over the same bandwidth produced by an LP PMD ADC with two-channel synchronizer.

The signal-to-noise ratio for the higher frequency case [Fig. 7(b)] is expectedly lower. First, the maximum signal amplitude is inversely proportional to the frequency since the LP PMD ADC is a delta modulator; it digitizes the signal derivative. For example, the maximum signal at 175 MHz is about 25 dB less than that at 10 MHz. Second, the signal-to-noise ratio is reduced further by the mixing of out-of-band quantization noise with the harmonics of the local oscillator. With a single-bit square-wave local oscillator, only odd harmonics are present and their powers decrease as $1/f^2$. On the contrary, the quantization noise power increases approximately as f^2, since the mixing occurs right after the delta modulator. For the example shown in Fig. 7, this excess noise is approximately 15 dB, corresponding to 31 odd harmonics of f_{LO} $(= f_{\mathrm{clk}}/128)$ of the

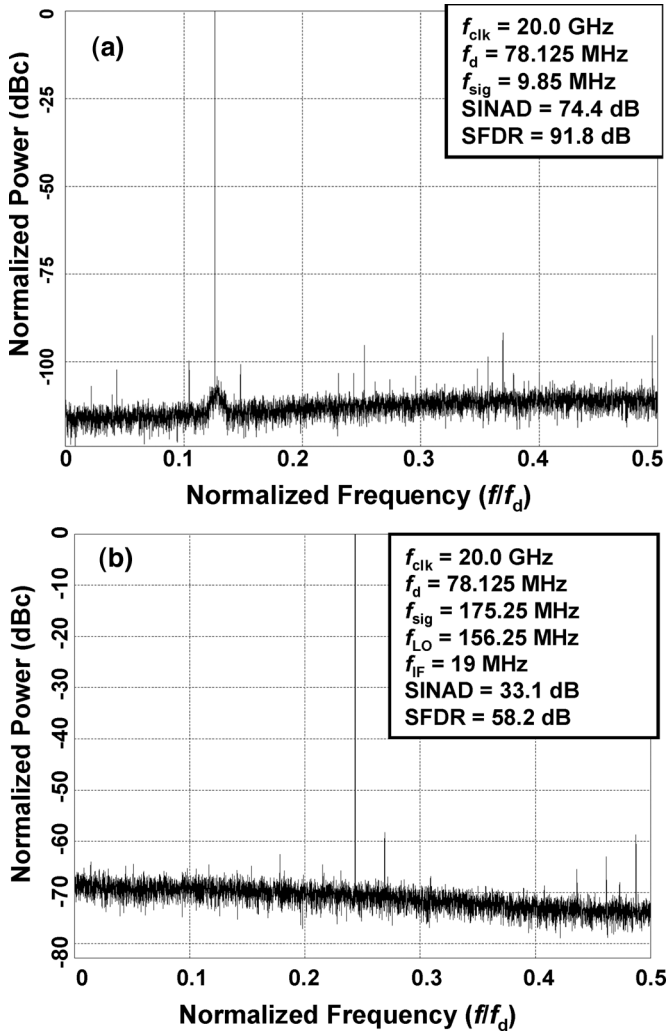

Fig. 7. Spectra (32768-point FFT) of the digitized output of the digital-RF receiver chip for input sinusoidal signals (a) 10 MHz signal without digital LO and (b) 175 MHz signal with digital LO.

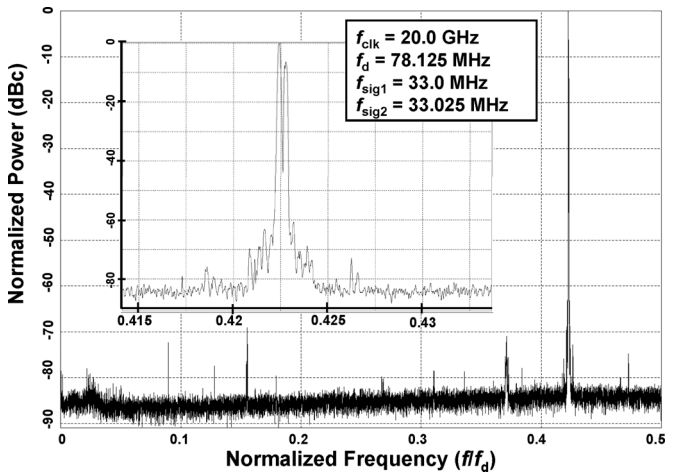

Fig. 8. Spectrum (32768-point FFT) of the digitized output of the digital receiver chip for two inputs at 33 and 33.025 MHz from two SINCGARS radios (courtesy: U.S.Army CERDEC) captured during a demonstration. The inset shows the zoomed region around the signal-of-interest.

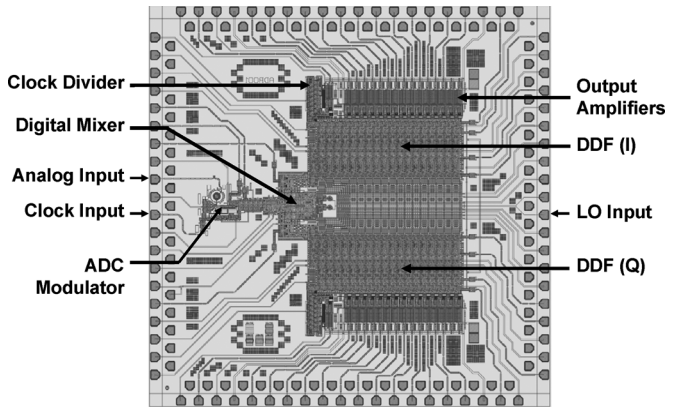

Fig. 9. Redesigned single-chip digital-RF receiver, comprising a digital channelizer with improved digital mixer and an LP PMD ADC, demonstrated better reliability.

local oscillator that fall within the unfiltered quantization noise band $0 - f_{\rm clk}/2$.

The digital receiver was also tested with signals from a pair of SINCGARS (single channel ground and airborne radio system) radios at different frequencies in the 30–88 MHz range. Fig. 8 shows the results of a test with two radio frequencies separated by the minimum permissible spacing of 25 kHz.

The next version of the lowpass single-chip digital-RF receiver (Fig. 9) was designed with the more robust digital mixer depicted in Fig. 4. This design is far less susceptible to bias current induced magnetic fields. Both filters work with identical bias values. Moreover, several chips from different locations on the same wafer and from different wafers demonstrated the same bias values and exhibited similar performance.

We measured this chip with our new room temperature interface amplifiers and PCI data acquisition and processing board. Fig. 10 shows the complex (I-jQ) FFT (8192 points) from the acquired I and Q data. The spectrum represents a bandwidth of $f_{\rm d} = {\rm f_{clk}}/256 = 55$ MHz.

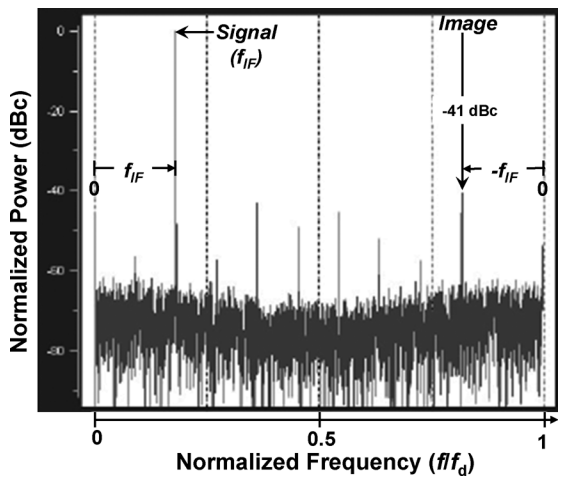

Fig. 10. Spectrum of the acquired digital I and Q data following complex FFT. The analog input sinusoidal signal of frequency 190 MHz is digitized by the lowpass ADC with fclk $=$ 14.08 GHz, digitally downconverted with fLO $=$ 180 MHz, and filtered to a decimated output bandwidth of 55 MHz.

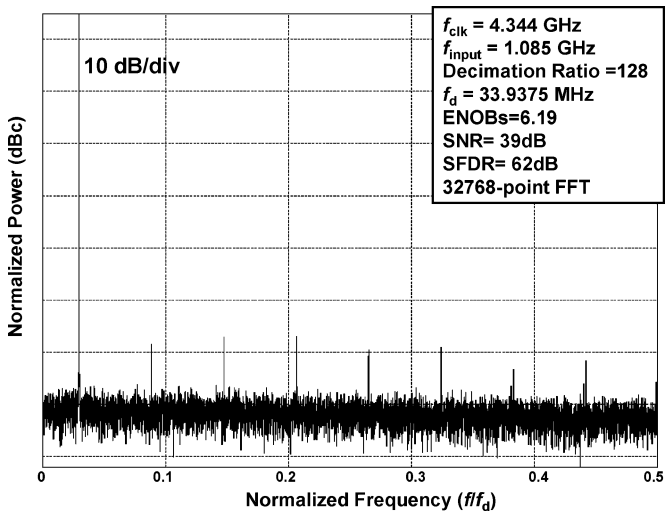

Fig. 11. Spectrum of digitized output of a first-order bandpass digital receiver with $\mathrm{fres} = 1.08\ \mathrm{GHz}$.

B. Bandpass Digital-RF Receiver

HYPRES has developed a family of bandpass delta-sigma (BP $\Delta\Sigma$) modulators to address the needs of various RF applications. These continuous-time BP $\Delta\Sigma$ modulators use an LC resonator to minimize quantization noise around the resonant frequency (f_{res}).

These bandpass ADCs have also been integrated with the digital channelizer. Ideally, the ADC sampling clock frequency should be $f_{\mathrm{clk}} = 4f_{\mathrm{res}}$. We have used this double-RF-oversampling for bandpass ADCs with f_{res} of 1.08, 4, and 5 GHz. Fig. 11 shows a typical spectrum for a first-order bandpass digital-RF receiver. If the required double-oversampling clock frequency is too high, one can use a lower clock frequency with some performance penalty. In this scheme, called RF undersampling, we take advantage of the sampling process that replicates the input analog frequency band, centered at f_{res}, translated by multiples of the sampling frequency (f_{clk}). In general, the sampled spectrum consists of an infinite number of band replicas at $\pm f_{\mathrm{res}} \pm n f_{\mathrm{clk}}$, where $\mathrm{n} = 0, 1, 2, \ldots$, but we are primarily interested in the first Nyquist zone $0 < f < f_{\mathrm{clk}}/2$. For $f_{clk} > f_{\mathrm{res}}$, the band center is shifted from f_{res} to $f_{clk} - f_{\mathrm{res}}$. We will need to apply a digital local oscillator at that frequency $(f_{LO} = f_{clk} - f_{\mathrm{res}})$ to mix it down to baseband. Furthermore, the local oscillator should be a submultiple of the clock frequency to prevent unwanted mixer artifacts, preferably by a factor divisible by 4 to ensure convenient generation of in-phase and quadrature components. The highest clock frequency under these constraints is given by $f_{clk} - f_{\mathrm{res}} = f_{clk}/4$, *or* $f_{clk} = 4f_{\mathrm{res}}/3$. Fig. 12 shows a single-chip X-band receiver that uses this RF undersampling approach. The delta-sigma modulator has a resonant frequency of 7.4 GHz and was clocked at 9.86 GHz. Since $f_{\mathrm{LO}} = f_{\mathrm{clk}}/4$, the clock was directly applied to the LO input of the mixer (Fig. 3).

Fig. 13 shows the result of 8192-point FFT of the acquired I and Q data from the X-band digital-RF receiver chip (Fig. 12).

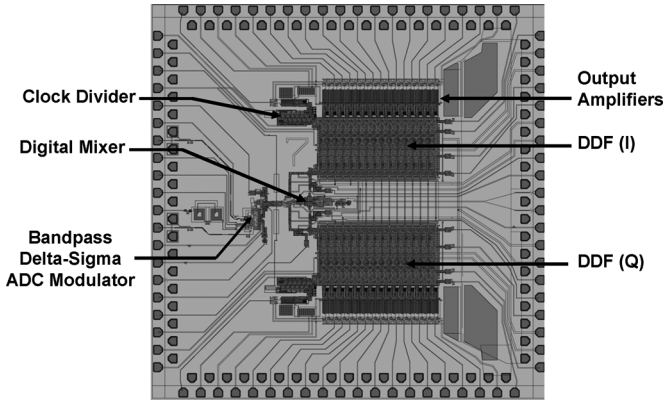

Fig. 12. Single-chip bandpass digital-RF receiver integrates a digital channelizer with a bandpass delta-sigma ADC modulator with $\mathrm{fres} = 7.4\ \mathrm{GHz}$.

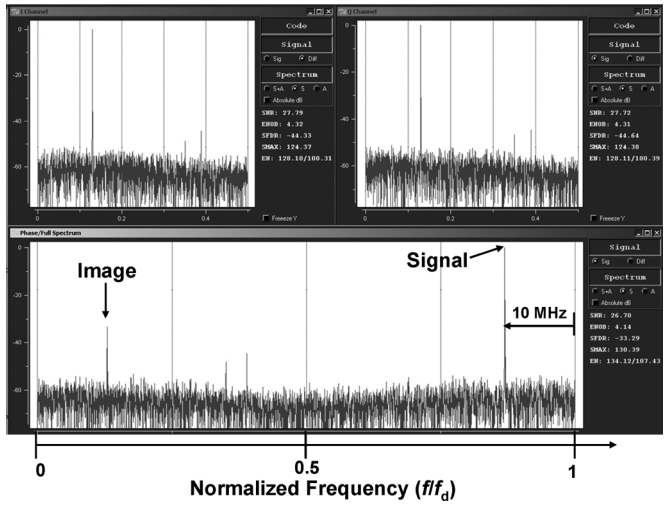

Fig. 13. Screen capture of our test graphical user interface shows the spectra of the I-channel output (top left), the Q-channel output (top right) along with the full spectrum ($\mathrm{I} + \mathrm{jQ}$, bottom). The analog sinusoidal input frequency is 7.402 GHz and the clock frequency ($\mathrm{fclk} = 4\mathrm{f}0/3$) is 9.856 GHz. The output bandwidth ($\mathrm{fd} = \mathrm{fclk}/128$) is 77 MHz.

This chip was extensively tested with modulated RF input signals produced by military satellite communication (MILSATCOM) equipment, including a modem, an analog frequency up-converter, and an analog frequency translator simulating the function of a satellite (Fig. 14). We have performed comprehensive testing with different modulation types over the entire range of operation of the modem. Fig. 15 shows the spectrum for offset quadrature phase shift keying (OQPSK) and 8 phase shift keying (8PSK) modulated RF signals, with the highest possible modulation rate of 6.5 Mbps from the modem.

C. Multi-Band Digital-RF Receiver

The modular and scalable digital-RF receiver architecture allows integration of multiple ADC modulators to multiple channelizers. We have designed a chip integrating a lowpass delta ADC and three bandpass delta-sigma ADC modulators with a single-phase digital mixer and a decimation filter as the first

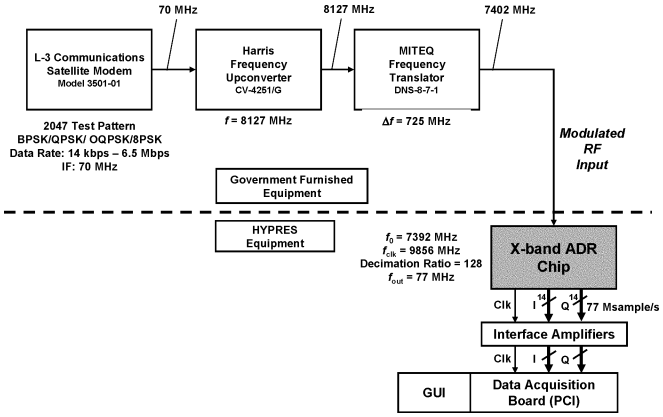

Fig. 14. Test configuration for the X-band ADR chip. Modulated RF signal with a carrier frequency of 7.402 GHz was applied to the input and the digitized I and Q data was captured for further analysis. All the equipment for production of the modulated RF signal was provided by U.S. Army CERDEC for testing at HYPRES.

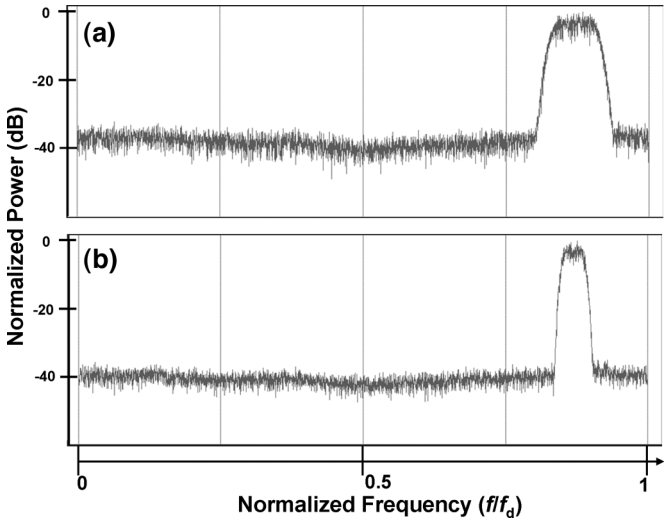

Fig. 15. Power spectrum of a modulated RF signals, (a) OQPSK and (b) 8PSK at 6.5 Mbps with a carrier frequency of 7.402 GHz, is applied to the X-band ADR chip. The clock frequency and the output bandwidth $(\mathrm{fd} = \mathrm{fclk}/128)$ are 9.856 GHz and 77 MHz respectively.

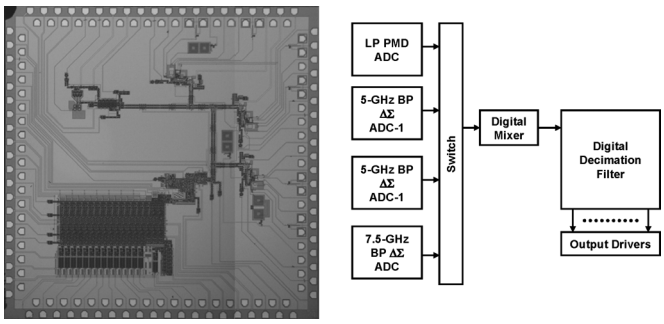

Fig. 16. Photograph (left) and block diagram (right) of a test chip with four different ADC modulators connected to a single mixer and filter.

step. This chip (Fig. 16) was fabricated with the 1 $\mathrm{kA/cm^2}$ process and tested at $f_{\mathrm{clk}} > 20$ GHz.

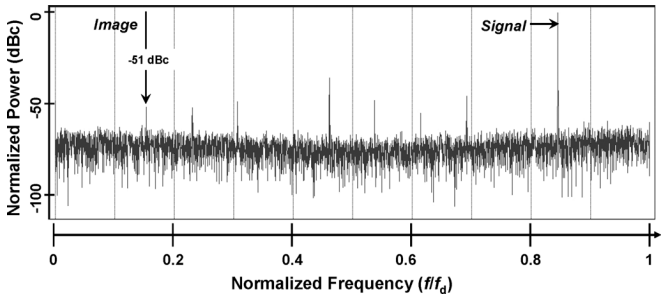

Fig. 17. Spectrum of the acquired digital I and Q data following complex FFT. The analog input sinusoidal signal of frequency is 190 MHz is digitized by the lowpass ADC with $\mathrm{fclk} = 16.64$ GHz, digitally downconverted with $\mathrm{fLO} = 180$ MHz, and filtered to a decimated output bandwidth of 65 MHz.

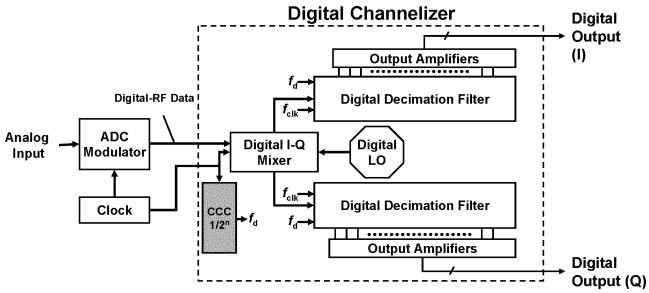

Fig. 18. Digital channelizer with a common clock controller (CCC) to ensure synchronicity between I and Q samples.

V. Digital Channelizer Improvements

A. Channelizer With Common Clock Controller

Ideally, complex downconversion eliminates the image frequency. In practice, one can judge the quality of the digital mixer by measuring the relative amplitude of the image signal. The image rejection of the channelizer (shown in Fig. 9) was measured from the complex FFT to be 41 dB (Fig. 10). Since the decimated clocks for the I and the Q filters are generated independently and locally near the two digital filters, they are not synchronized to each other. Any time shift between I and Q output samples manifests itself by increasing the amplitude of the image signal. By adjusting the time shifts between the two filters, one can occasionally get better performance, as illustrated by the spectrum (Fig. 17) of 8192-point I and Q data. The image rejection for this particular acquisition is 10 dB better than the typical one shown in Fig. 10. Therefore, we designed a common clock controller (CCC) with clock distribution network to ensure synchronization between the I and the Q outputs (Figs. 18 and 19).

The common clock controller comprises a single frequency divider, augmented by additional synchronization circuitry (D-flip-flops clocked by the master clock) to ensure that the clock streams at different decimated frequencies maintain the timing accuracy of the master. The clock distribution network was designed to maintain equal propagation delays of the decimated clock (f_{d}) to both DDFs. With this new design, we observed over 50 dB image rejection consistently (Fig. 20).

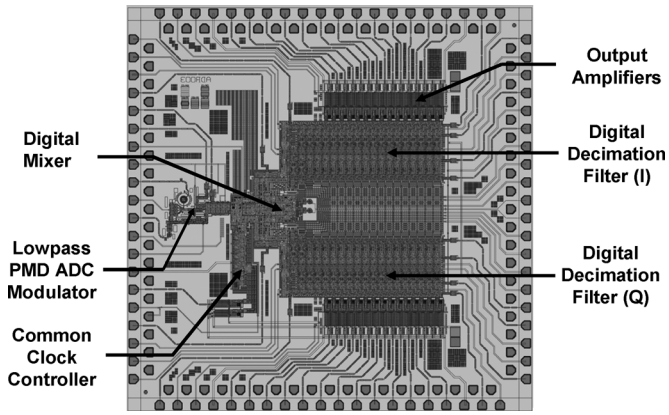

Fig. 19. Improved single-chip digital-RF receiver employing a common clock controller for generation of all timing signals from a single frequency divider.

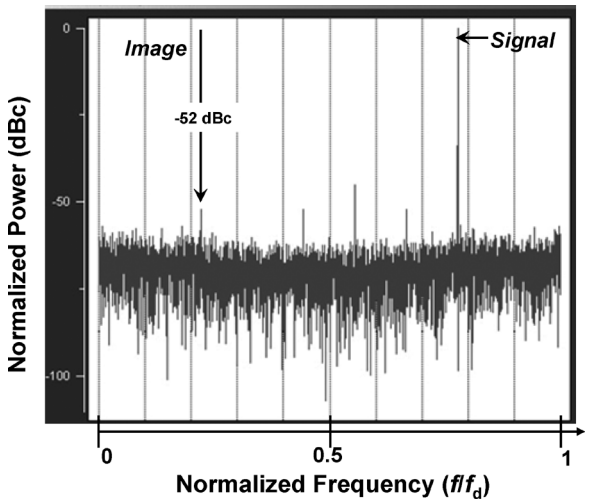

Fig. 20. Power spectrum of the acquired digital I and Q data following complex FFT. The analog input sinusoidal signal of frequency is 190 MHz is digitized by the lowpass ADC with fclk $= 11.52$ GHz, digitally downconverted with fLO $= 180$ MHz, and filtered to a decimated output bandwidth of 45 MHz.

The common clock controller is located close to the digital mixer (Fig. 19) and requires considerable ($\sim$100 mA) bias current. In spite of this no adverse effect on the mixer operation was observed, further validating its ground-current immunity.

B. Channelizer With Serialized Outputs

Another improvement, pursued in parallel, is to reduce the number of output lines from a channelizing receiver through serialization. This improvement is an essential step towards realization of a cryocooled multi-channel digital-RF receiver. Reduction of the number of high-speed digital data links between the 4-K stage of a cryocooler and room temperature is necessary for minimization of the cryocooler heat load, an essential step towards miniaturization of such receivers and transceivers.

Since serialization increases the output data rate ($f_{\rm s} = 2^{\rm m} f_{\rm d}$) by the serialization factor, the performance of the on-chip output drivers and the interface amplifiers at higher temperature become critical. In our design, we use decimation ratios of 256 and 512 for the 1 $\rm kA/cm^2$ ($f_{\rm clk} = 20$ GHz) and 4.5 $\rm kA/cm^2$

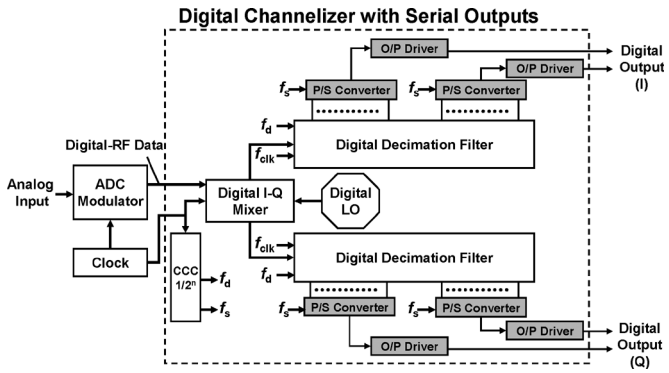

Fig. 21. Digital channelizer with parallel-to-serial (P/S) converters attached at the DDF output.

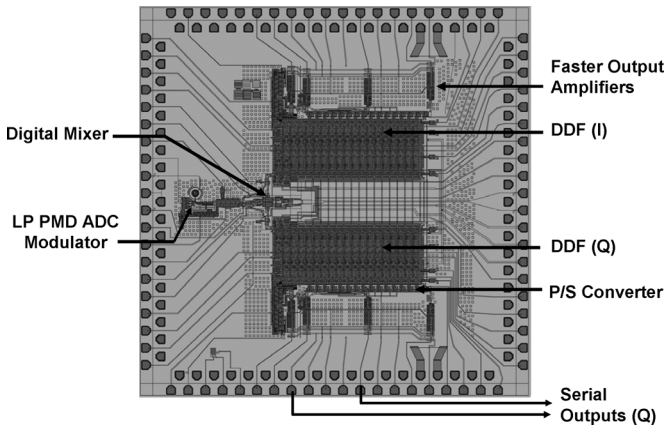

Fig. 22. Single-chip digital-RF receiver with serialized outputs.

($f_{\rm clk} = 40$ GHz) versions respectively, maintaining the maximum decimated clock rate of $f_{\rm d} = 78.125$ MHz. Although our on-chip drivers and interface amplifiers were designed to support rates up to 1.3 GHz, enough for full serialization of a 16-bit DDF output, so far we have adopted a more conservative design with two 8:1 parallel-to-serial converters, for a maximum output rate $f_{\rm s} = 625$ MHz. Fig. 21 shows a block diagram of the channelizer with serial outputs.

To validate this approach, we designed and tested an ADC chip with serialized outputs [11]. This serial-ADC chip includes an identical LP PMD ADC front-end attached to a single decimation filter with serial output. We have demonstrated successful operation of a 4.5 $\rm kA/cm^2$ serial-ADC chip at $f_{\rm clk}$ above 30 GHz. This chip allowed us to optimize both the internal timing on chip, and the room temperature interface, containing fast SiGe amplifiers and deserializers.

The initial design of the serialized single-chip receiver without a common clock controller is depicted in Fig. 22. The spectrum of down-converted and filtered data from this chip with $f_{\rm clk} = 6.4$ GHz is shown in Fig. 23. We have tested several of these chips and observed correct serialized outputs. However, excess noise on the voltage waveform at the driver output, probably arising from errors in the filter and/or output drivers, has prevented data acquisitions at high clock speed so far. The measured signal-to-noise ratio is commensurate with results from the parallel-output design (Figs. 6 and 7) after

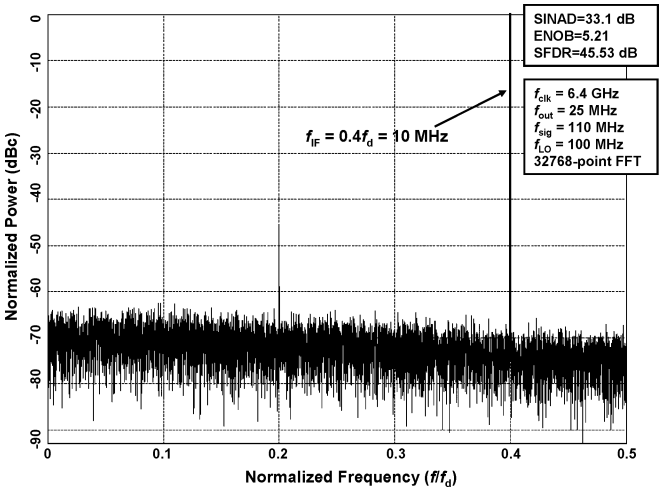

Fig. 23. Spectrum (32768-point FFT) of the digital-RF receiver chip with serial output.

taking into account lower f_{clk}, and different signal (f_{sig}) and local oscillator (f_{LO}) frequencies.

We have also designed, but have not yet fully evaluated, digital-RF receiver chips that include a common clock controller and parallel-to-serial converters, with both LP PMD ADC and BP $\Delta\Sigma$ ADC front ends.

VI. Conclusion

We have successfully demonstrated a digital channelizer circuit, containing more than 10,000 Josephson junctions. This circuit has been integrated with lowpass and bandpass ADCs to demonstrate, for the first time, a set of single-chip digital RF receivers.

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