Two-Phase 50 GHz On-Chip Long Josephson Junction Clock Source

Igor V. Vernik and Deepnarayan Gupta

***Abstract*— On-chip, high-frequency clock sources are essential for the future development of superconductor digital circuits and systems. We have developed clock sources for rapid single flux quantum (RSFQ) digital circuits using high-quality long Josephson junction (LJJ) resonant oscillators that offer extremely low jitter. To meet the requirement for time-interleaved clock signals of complementary phase, two-phase 30 and 50 GHz clock sources using LJJs have been developed with both linear and annular geometry. Unperturbed by reflections from boundaries and collisions among the fluxons (flux quanta), the annular LJJ oscillator has demonstrated superior stability and higher quality factor (>10^6) than the linear LJJ oscillator. The LJJ oscillator with linear geometry is easier to interface with RSFQ circuitry since it has well-defined boundaries at either end, facilitating a two-phase clock source. On the other hand, multiple clock phases may be derived from an annular LJJ oscillator by connecting interface circuitry at various points around the circular junction, if the interface circuitry does not interfere with the fluxon(s) in the annular junction. Experimental results for two-phase RSFQ clock sources based on linear and annular LJJ oscillators are presented.**

***Index Terms*—On-chip high frequency clock source, long Josephson junction, superconductor digital electronics.**

I. Introduction

The prospect of cryogenic superconductor digital electronics is encouraging for a number of commercial and military applications, where its advantages in high speed (10-100 GHz), low power consumption (~mW per chip) and quantum accuracy are superior to other technologies. Almost all superconducting digital electronics require a clock signal in the 10-100 GHz range. External clock generators capable of such high frequency are very expensive and require extensive waveguides and transmission lines, which makes a dominant contribution to the thermal load on the cryogenic system by conducting heat from room temperature. In spite of significant advances in closed-cycle refrigerators in the past two years, the major hindrance to introduction of superconductor electronics in a range of products, such as wideband radios for wireless communications, high-speed network switches and routers, remains the cost and complexity of the cryogenic support system. An on-chip high-frequency clock source eliminates the need for expensive external generators, while diminishing the system power requirements by reducing the thermal load.

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A. Long Josephson Junction Oscillators for Superconductor Electronics

Among various on-chip clock sources for superconductor electronics, we have chosen an oscillator based on resonant soliton modes in a long Josephson junction (LJJ). A long Josephson junction refers to a two-dimensional geometry, which is much larger than the Josephson penetration depth (λ_J) in one dimension and much smaller in the other [1]. A fluxon (or a magnetic flux quanta, $\Phi_0 = h/2e$) in an underdamped LJJ of a conventional linear geometry traveling back and forth between the two ends along the long dimension of the junction has the properties of a soliton.

In zero or relatively weak magnetic field, a soliton (or fluxon) propagating in one direction reverses direction upon hitting the end of a linear LJJ, changing the quantum mechanical phase at the junction boundary by 4π. Due to low losses in underdamped LJJs this process is repeated resulting in the resonant (back and forth propagation) soliton mode. As external magnetic field increases, magnetic flux penetrates into the junction. The fluxons are introduced at one end and are accelerated towards the other end by the junction bias current. This unidirectional flow of flux is called the flux-flow mode.

A high-frequency oscillator can be realized using both the resonant and flux-flow soliton modes, since soliton – an electromagnetic pulse – impinging on a junction boundary, gives rise to the emission of pulse of electromagnetic energy. If the arrival of solitons at one end of the junction is periodic, an *rf* radiation is emitted. An oscillator using the resonant soliton mode has a very narrow linewidth and small power, while an oscillator using the flux-flow mode has a broader linewidth and larger power.

Since the applied magnetic field is zero or small, the oscillator frequency in the resonant mode is determined primarily by the junction length (L), implying a rather well defined frequency. The resulting resonant step in the I-V characteristic is commonly called a *zero field step* (ZFS). When the LJJ is biased on a zero field step, the emitted radiation is characterized by a very narrow output linewidth. The modified Josephson relation gives the frequency f of a resonant soliton oscillator:

$$f = V_{dc}/2\Phi_0 = nu/2L, \qquad (1)$$

where *u* is the average fluxon velocity, and *n* is the number of fluxons (and anti-fluxons) moving in the junction of length *L*. For the flux-flow mode output frequency is tunable since it depends on external magnetic field and bias current.

The strong dependence of the resonant frequency on the applied magnetic field, another source of fluctuation, broadens the spectral linewidth of a flux-flow oscillator. Although the resonant soliton oscillator power is smaller, it is adequate for clocking rapid single flux quantum (RSFQ) digital circuits. The RSFQ technology is based on the propagation of a fluxon in a circuit, where digital "1"("0") corresponds to the presence (absence) of the fluxon with respect to a clock. Therefore, the timing of the clock pulse, also in the form of a fluxon, is very important. The clock signal needed by an RSFQ logic gate is a periodic train of single flux quantum (SFQ) pulses. This SFQ pulse train for RSFQ circuits is derived by coupling an LJJ oscillator to an interface circuit. It consists of specially designed Josephson transmission line (JTL) stages in such a way that the first JTL stages in the interface were designed to have the largest possible inductance to minimize loading the resonant oscillators.

TABLE I
COMPARISON OF DIFFERENT JOSEPHSON JUNCTION OSCILLATORS

OSCILLATOR TYPE	QUALITY FACTOR ($f/\Delta f$)	TYPICAL FREQUENCY
Single small junction	100 - 1000	> 100 GHz
Array of small junctions	10^3-10^4	> 100 GHz
Long junction in flux flow mode	~10^3	> 100 GHz
JTL ring oscillator	1000 - 5000	10 – 20 GHz
Long junction in resonant mode	10^5 – 10^6	10 – 100 GHz

Table 1 shows a comparison of different Josephson junction oscillators for RSFQ electronics. Usually, the higher the quality factor, the lower is the time jitter of the corresponding clock signal. The accuracy of large scale digital circuits, e.g. data conversion devices like analog-to-digital, digital-to-analog, and time-to-digital converters depends on the quality of the clock source, especially at very high (>10 GHz) clock speeds, which is the realm of superconductor electronics. RSFQ clock sources based on LJJ resonant oscillators have demonstrated Q greater than 10^6 [2] and a time jitter of 50 fs [3].

B. Linear and Annular Long Josephson Junction Oscillators

We have demonstrated RSFQ clock sources based on LJJ resonant oscillators with both linear and annular geometries [4]. For both geometries, the first zero field steps have been measured. Figure 1 shows current-voltage characteristic of the annular LJJ with one trapped fluxon. The annular LJJ is a topologically closed system such that the number of trapped fluxons is conserved and new fluxons can be created only in the form of fluxon–antifluxon pairs. This is reflected by the appearance of the 3rd step in Fig.1 (one fluxon-antifluxon pair is created in addition to the one trapped fluxon). The annular LJJ acts as clock source with the frequency of 50 GHz if it is biased on the first step with the voltage of 100μV.

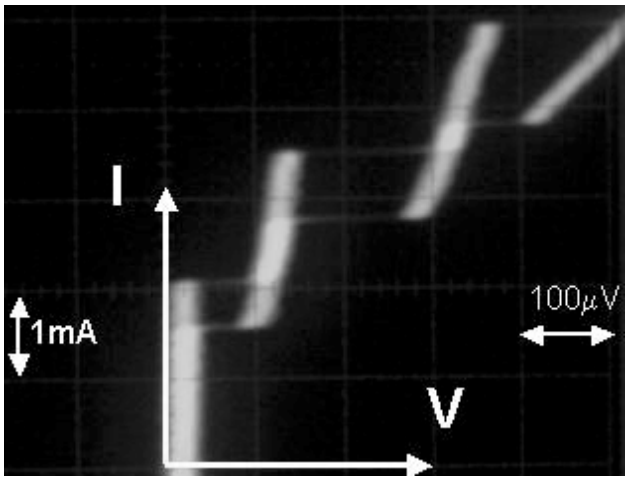

Fig. 1. The current-voltage characteristic of the annular LJJ with one trapped fluxon shows the 1st and the 3rd steps.

II. DESIGN OF TWO-PHASE CLOCK SOURCE

In most RSFQ applications, two time-interleaved streams of clock signals are required to provide alternate clocking of two parts of a circuit. In the past, these two clock streams were derived from a single master clock source using a complementary output toggle flip-flop; the resultant clock streams being at half the frequency of the master clock source. The LJJ oscillator with conventional linear geometry provides two complementary clock streams of the same frequency from its two ends, which are exactly 180 degrees out of phase. The LJJ oscillator with linear geometry is easier to interface with RSFQ circuitry since it has well-defined boundaries at either end, facilitating a two-phase clock source. On the other hand, multiple clock phases may be derived from an annular LJJ oscillator by connecting interface circuitry at various points around the circular junction. However, in the absence of well-defined boundaries in an annular LJJ, coupling interface JTLs at multiple points on the annular LJJ could have an adverse effect on the resonant oscillations.

Figures 2a and 2b show the layouts of a linear and an annular LJJ oscillator coupled to two chains of binary frequency dividers through two interface JTLs on either end. The first JTL stages in the interface were designed to have the largest possible inductance to minimize loading the resonant oscillators. In order to apply weak external magnetic field control lines are designed on top of LJJ oscillators – the Nb strip is fabricated on top of linear LJJ and one-turn Nb coil is placed coaxially with annular junction [5]. The linear junction is 110 μm long and the annular junction has a mean radius of 40 μm and a width of 5 μm. The chips with LJJ oscillators interface JTLs and 8-bit binary counter have been fabricated using standard HYPRES 3 μm 1kA/cm^2 process [6].

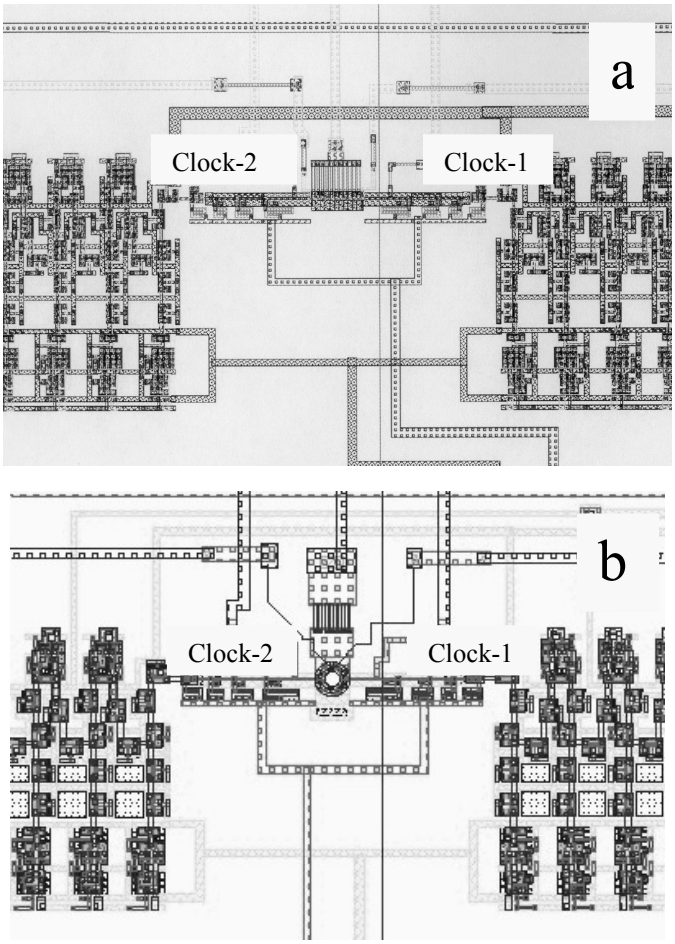

Fig. 2. The layouts of (a) linear and (b) annular LJJ oscillator coupled through two interface JTLs to two chains of binary frequency dividers (only first two dividers are shown for the clarity) on both ends.

The linear LJJ produces two SFQ pulses at each boundary, corresponding to a 4π phase rotation. Therefore, the output frequency is $2f_0$, where $f_0 = \bar{c}/2L$ and $\bar{c}$ is the Swihart velocity [1]. The annular junction does not have a boundary and only one SFQ pulse is produced in a JTL coupled to it, corresponding to a 2π phase rotation. Therefore, the output frequency is $f_0 = \bar{c}/2\pi r$, where r is the mean radius of the annular LJJ.

III. EXPERIMENTAL RESULTS

Two phase clock streams produced by both linear and annular oscillators were measured from the digital outputs from the eighth and the ninth stages of the binary frequency divider. Figures 3a and 3b show the block diagrams of the two clock generator circuits. The chain of toggle flip-flops (TFFs) not only provides a set of digital clock streams at different binary sub-harmonics of the oscillator but also is useful for producing a selectable clock source [2].

The digital outputs for display were obtained using TFF-type SFQ/DC converters that convert SFQ pulses into transitions of a voltage waveform of ~250 μV amplitude, which was subsequently amplified at room temperature. MITEQ amplifier models No. AU-1332 and No. AM-1431 with 0-500MHz and 0-1GHz bandwidth and gain 46dB and 37dB respectfully have been used. A wideband four-channel digital oscilloscope (Tektronix TDC 694C) was used to display the waveform and calculate its frequency.

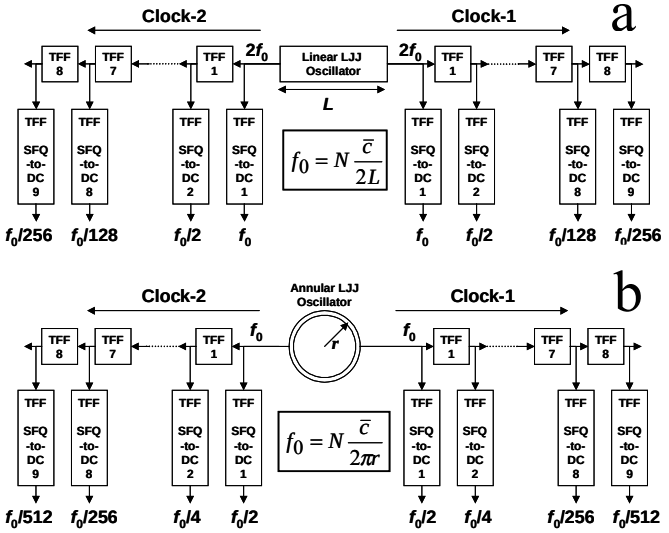

Fig. 3. Block diagram of the two phase clock generator using (a) linear and (b) annular LJJ.

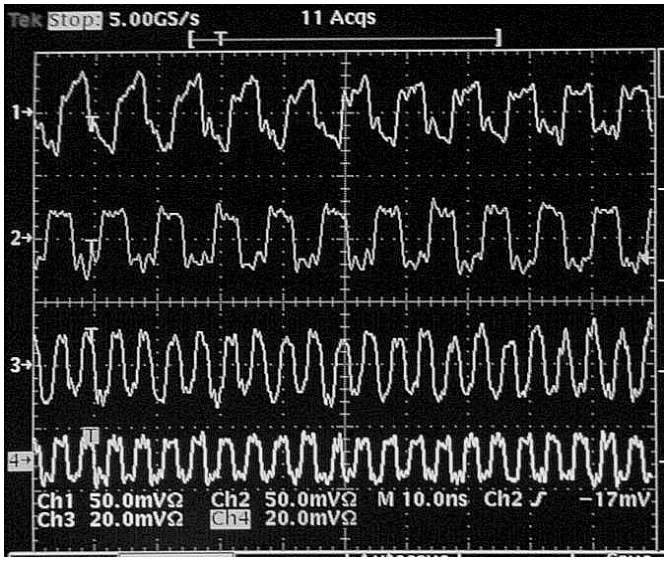

Fig. 4. The waveforms of four outputs from linear LJJ. The frequencies are the following: output 1 – 111.11 MHz, output 2 – 113.63 MHz, output 3 – 221.42 MHz, output 4 – 227.27 MHz. LJJ is biased on the first ZFS.

Figure 4 shows the two digital clock outputs from the last two stages of the frequency divider chain from each side of the linear LJJ oscillator, biased on the first step. Figures 5a and 5b show the same outputs for an annular junction. In all these cases, the outputs 1 and 3 are from the Clock-1 side; the outputs 2 and 4 are from the Clock-2. For the outputs 1 and 2, the output frequency is divided by 2^9 and the signal is amplified by 37 dB. For the outputs 3 and 4, the output frequency is divided by 2^8 and the signal is amplified by 46 dB. The clock frequency f_0 was calculated to be 28 GHz and 33 GHz for the linear and the annular LJJ oscillator, respectively.

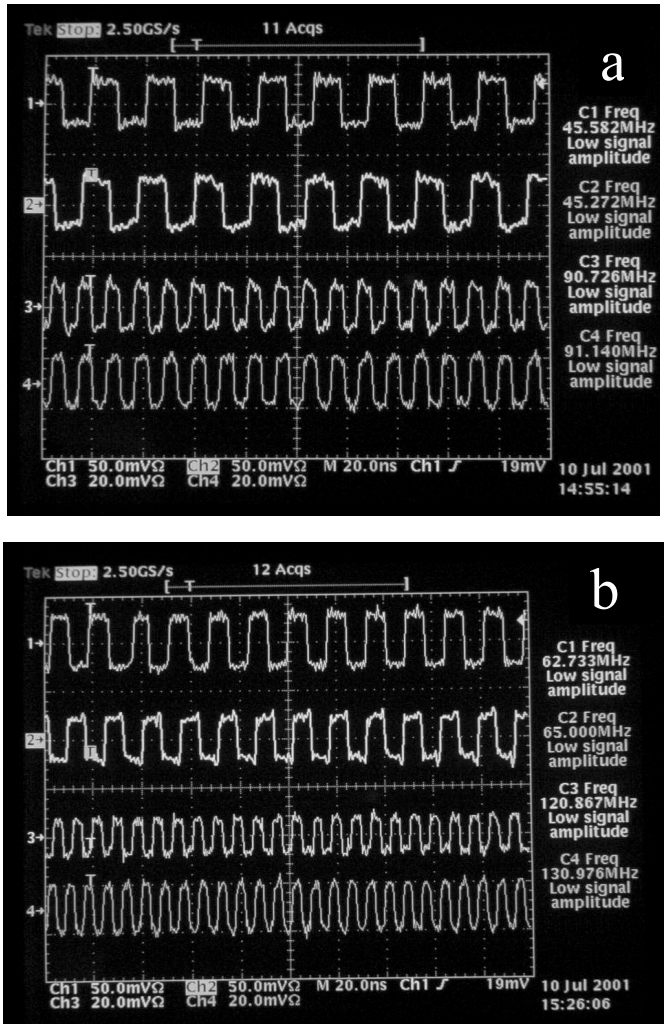

Fig. 5. The waveforms of four outputs from annular LJJ. LJJ is biased on the first ZFS with (a) 2.31mA current and (b) 4.2mA current, corresponding to the bottom and the top of the ZFS respectively.

We found a difference in the clock frequencies between the two phases, especially in the case of the annular LJJ. Figure 6 shows the current-voltage characteristics of the annular LJJ, reconstructed from the frequency measurements. The frequency difference between the two clock phases is about 5% and 2% in the case of the annular and the linear LJJ respectively. Since the difference was more pronounced near the top of the step, where the frequency is the highest, we believe that this discrepancy reflects the statistics of occasional failure of the frequency divider chain, most likely the first TFF that is subject to the highest frequency. In this design, all the TFFs share a common bias. The easiest way to overcome this problem is to use a separate designated bias line for the TFF closest to the LJJ oscillator [8]. The design has been changed to incorporate this improvement and modified chips are being fabricated and measured.

From this measurement, not only we were able to calculate the frequency (f_0) of the LJJ clock, but also reconstruct the current-voltage characteristics of the zero field step (Fig. 6). Compared with the traditional approach of measuring the junction voltage, this is more accurate, and more relevant for the utilization of the oscillator as a clock source for RSFQ circuits. The linewidth Δf of the oscillator may be calculated using the thermal noise model [7]:

$$\Delta f = (4\pi k_B T / \Phi_0^2)(R_d^2 / R_s), \qquad (2)$$

where k_B=1.38 x 10^{-23} J/K is the Boltzmann's constant, Φ_0 = 2.07 mV·ps is the magnetic flux quantum, R_d and R_s are the differential and *dc* resistance at the operating point, respectively. For the 33 GHz annular junction, biased at 4 mA, the quality factor Q (= $f/\Delta f$) was calculated to be 4.35×10^5 at f = 33.3 GHz using (2). This is slightly smaller than previously reported values [2].

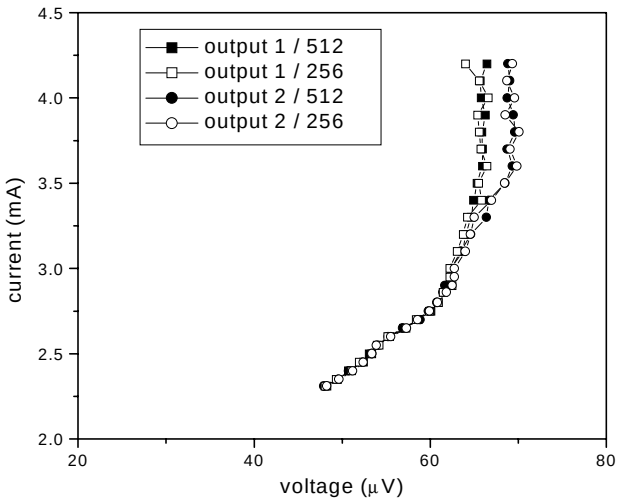

Fig. 6. The first zero-field step of the current-voltage characteristics of the annular LJJ, reconstructed from the frequency measurements.

IV. CONCLUSIONS

Clock sources with frequencies of 30 and 50 GHz for the superconductor digital circuits have been developed using long Josephson junction oscillators in resonant mode. Two clock streams with complementary phases were obtained from the LJJ oscillators with both linear and annular geometry. Such a two-phase clock source is extremely useful for clocking a variety of RSFQ digital circuits, where time-interleaved clocking of different circuit components is required.

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