Parametric Testing of HYPRES Superconducting Integrated Circuit Fabrication Processes

Daniel Yohannes, Alex Kirichenko, Saad Sarwana, and Sergey K. Tolpygo

***Abstract*—A set of diagnostic chips for process control and design parameters evaluation has been developed for HYPRES' 1.0kA/cm^2, 4.5 kA/cm^2, and 20 kA/cm^2 fabrication processes, consisting of four 5 × 5-mm chips. Testing was performed on automated test setup (OCTOPUX) that automatically logs results and maintains records of fabrication process and design parameters. The design of diagnostic structures and automated testing algorithms are discussed. Statistical data are presented on the uniformity and run-to-run variation of the critical currents, critical current density, junction size, inductances, and other fabrication and design parameters collected since September 2005. The influence of the fabrication parameters deviation on operational margins and yield of large superconducting digital integrated circuits is discussed, as well as requirements for the 20kA/cm^2 (80 GHz) process.**

***Index Terms*—Critical current, Josephson device fabrication, Josephson junction, sheet inductance, sheet resistance, statistical process control, superconducting integrated circuits.**

I. Introduction

DESPITE the unparalleled advantages of superconducting digital electronics in speed and power consumption, the integration level of superconducting integrated circuits (SICs) is still very low in comparison with semiconductor ICs. Although there has been some slow and steady growth of complexity of SICs, the typical superconducting digital circuits operating at about 20 GHz clock frequency contain only about $6 \cdot 10^3$ Josephson junctions (JJs) per chip [1]. The low level of integration dramatically limits the functionality of SICs and thus impedes progress and penetration of superconductor electronics to the market.

Current restrictions on the integration level are coming from both the fabrication and design. From the fabrication side, the circuit complexity is limited by the maximal size of a yieldable circuit, i.e., by available equipment and processes. To address this issue, in early 2004 we completed an upgrade of HYPRES fabrication facilities, equipment, and fabrication processes. This allowed us to quickly double the complexity of our SICs by increasing the number of Josephson junctions per chip to about $1.3 \cdot 10^4$, and increase the clock frequency to above 30 GHz [2], [3].

Manuscript received August 29, 2006. This work was supported in part by ONR.

The authors are with HYPRES Inc., Elmsford, NY 10523 USA (e-mail: daniel@hypres.com; alex@hypres.com; sarwana@hypres.com; stolpygo@hypres.com).

Digital Object Identifier 10.1109/TASC.2007.897399

In order to have a healthy progress in the industry, the integration level of SICs and the clock frequency need to keep growing. This brings to the forefront the issues of yield, manufacturability, and process control and monitoring as it has long been recognized by the semiconductor industry. Superconducting IC fabrication is currently, of course, at a much less advanced stage than the semiconductor one, but the need in a tight process control and characterization has been recognized and implemented to various degree of sophistication by all foundries, e.g., [4]–[8]. Both the design and fabrication parameters have to be monitored and controlled to insure a stable process. Similarly to a very large-scale integrated circuit fabrication in semiconductor industry, this has been achieved by implementing process control monitors (PCMs). Since the superconducting IC fabrication is in many respects similar to the semiconductor IC manufacturing as far as the tools and processes are concerned, the design of PCMs can use many elements and test structures similar to those implemented in semiconductor industry, e.g., for linewidth control, dielectric integrity, defect screening, etc. [9], [10]. Superconducting nature of the circuits requires adding only a few specific structures.

In this paper we describe the parameters under control in the HYPRES superconducting IC fabrication processes [11]–[13], the test structures, automated test and data collection algorithms, and give a summary of PCMs test results collected since September 2005. A set of diagnostic PCM chips with test structures enabling the extraction of required parameters has been placed in five representative locations across wafers. The locations have been kept the same from run-to-run to monitor wafer-to-wafer variations.

II. Process and Circuit Parameters

Digital superconducting electronics implements Josephson junctions (JJs), resistors, inductors, and interconnects as circuit elements. HYPRES' superconducting IC fabrication processes are based on Nb/AlOx/Nb Josephson junctions. Fabrication processes are classified by Josephson critical current density j_c, a property of the $\mathrm{Nb/AlO}_x\mathrm{/Nb}$ trilayer. Presently, HYPRES foundry supports a low (30 A/cm^2) and medium (1.0 and 4.5kA/cm^2) critical current density processes [11]. High-j_c (20 kA/cm^2) process is currently under development [12].

The typical 150-mm wafer contains over $5{\cdot}10^5$ JJs and can be populated by 508 chips with 5 mm × 5 mm die size. To meet the increasing demand in IC's complexity, HYPRES devotes a part of the wafer to chips with 10 mm × 10 mm die size. Compared to two years ago, there has been a three-fold increase in the number of 10-mm chips on the typical HYPRES wafer. The 5-mm chips usually contain up to 2000 JJs whereas the 10-mm

chips typically contain up to 13000 JJs. On average JJs cover about 1% of the total wafer area.

A. Josephson Junctions

The minimum set of parameters required for circuit design and characterization of JJs includes the critical current (I_c), physical area (A), normal state resistance (R_N), sub-gap resistance (R_{sg}) defined as the resistance at 2 mV, specific capacitance (C_s), gap voltage (V_g); and secondary parameters such as the I_cR_N product and characteristic voltage $V_m = I_cR_{sg}$. These parameters are extracted by testing 20-junction arrays of unshunted junctions of various sizes ranging from 1 μm to 4 μm in diameter (30 μm for the low-j_c process); circular junctions are implemented. The critical current density and the size bias (missing radius dr) are extracted by fitting the data to $I_c = j_c\pi(r - dr)^2$ [11]. Since the critical (switching) current of small-unshunted junctions can be affected by thermal and external noise, 100-junction arrays of critically damped ($\beta_c = 1$), shunted junctions of various sizes were also implemented for complementary extraction of j_c and dr.

A room temperature electric test of the junction normal resistance was also done by measuring the difference of the resistance of a 100-junction array and the resistance of the same array structure without junctions (only the base electrode, wiring, and contact holes remaining). Arrays of different JJ sizes were used. A good proportionality between the junction normal conductance G_N at room temperature and the Josephson critical current density at 4.2 K was found as it could be expected from the Ambegaokar-Baratoff relationship for I_cR_N. The experimentally determined j_c/G_N ratio was used for a quick screening of wafers from these room temperature measurements. Specific capacitance C_s was extracted from the plasma resonance in large Josephson junctions [14].

B. Resistors

Resistors are needed for JJ shunting, circuit biasing and impedance matching. On average, resistors cover about 1.5% area of the wafer. For the medium current density process, sputtered molybdenum film is used as a resistor layer; $\mathrm{MoN_x}$ is used for 20 $\mathrm{kA/cm^2}$ process [12], and nonsuperconducting Ti/PdAu/Ti multilayer is used for the 30 $\mathrm{A/cm^2}$ process. For thin-film resistors, $\mathrm{R = R_{sq}N_{sq}}$, where $\mathrm{R_{sq} = \rho/d}$ is the sheet resistance (resistance per square) and d is the film thickness. $\mathrm{N_{sq}}$ is the effective number of squares that includes the geometric factor $l/(w + dw)$, the contribution of corners, and spreading resistance associated with contact holes. Here, l and w are the resistor length and width, respectively; dw is the deviation of the resistor linewidth from the design value (bias) due to lithography and etch processes. All these parameters were extracted from four-probe strip configurations ($l \gg w$) of different widths and meander-shaped resistors. An additional large-size square or cross-type geometry was used to check $\mathrm{R_{sq}}$ independently from Van der Pauw-type measurements [15].

C. Inductors

There are four niobium superconducting layers in the HYPRES processes: ground plane M0, junction base electrode M1, the first wiring layer M2, and the second wiring layer M3. Five inductor configurations are being used in circuits and have been studied: M1 over M0 ground plane, M1 sandwiched between M0 and M3 ground planes; M2 over M0 ground plane, M2 sandwiched between M0 and M3 ground planes; M3 over M0 ground plane.

Similar to resistors, an inductor can be parameterized by its sheet inductance L_{sq} (an inductance per square). The sheet inductance depends on the effective magnetic field penetration depth of the superconducting films and the thickness of the dielectric between the film and the ground plane. The inductance of a long strip over the ground plane is well approximated by

$$L = L_{sq}l/(w + b) \tag{1}$$

where l is the strip length, w is its width and b is a combination of the width bias and a fringing factor that characterize 3-D distribution of the magnetic field at the sides of the strip line. Whereas parameter b is necessary for circuit design purposes, the sheet inductance allows for monitoring the quality of niobium films. To measure the inductance of a strip line, the flux-voltage characteristics of dc-SQUIDs are used. The parameters L_{sq} and b are extracted by measuring the inductances of strip lines of different width and length, and fitting the experimental data to (1).

D. Interconnects and Contacts

Niobium thin film wires are used for interconnecting circuit elements; the interconnections can be formed in any of the four superconducting layers. The following parameters are monitored for the superconducting layers: critical temperature $\mathrm{T_c}$, critical current per unit width of the wire, and the linewidth bias extracted from electric measurements in the normal state. The critical current of wires depends on the layer surface topography and reduces if the wire crosses over edges of underlying structures. Resistance measurements on meander- and comb-type structures are used to monitor the lithography and etch processes at the minimum allowed line spacing as well as particulate defects causing shorts between the lines [9].

Different layers are connected to each other by using contact holes. There are three types of contact holes between the four superconducting layers, labeled as I0 (between layers M1 and M0), I1B (between M1 and M2, between resistor layer R2 and M2; and between junction counter electrode layer I1A and M2), and I2 (between layers M2 and M3). The largest HYPRES circuits contain about $6 \cdot 10^4$ I1B contact holes.

Contacts between nonadjacent layers (e.g., M2 to M0) are formed using vias presenting several contact holes placed on top of each other (e.g., I1B over I0). Patches of corresponding intermediate metal layers are needed (e.g., M1 in the example above) to achieve high superconducting critical currents of vias.

The critical current of all types of the contact holes and vias of the minimum size allowed by the Design Rules was monitored using arrays of 10,000 contact holes for I0 and I2, and 30,000 I1B contact holes. A quick characterization of the contact holes lithography and etch processes was also done by room temperature resistance measurements.

E. Interlayer Dielectric (ILD)

Silicon dioxide deposited by low temperature Plasma Enhanced Chemical Vapor Deposition (PECVD) is used as an ILD. Four SiO_2 layers are needed to insulate five metal layers. The main parameters that are monitored are the ILD thickness and specific capacitance. The thickness was measured using a *Tencore P-10* profilometer and a *Gartner* ellipsometer; plane capacitors between various metal layers were used for specific capacitance measurements. Another parameter of the prime importance is the ILD integrity and step coverage. It was monitored by checking for electric shorts between wires in different layers placed over different topographies such as a meander over a plane, a meander in one metal layer crossing over meanders in one or several different metal layers, a meander in one metal layer going along the edge of a meander in a different metal layer.

III. PCM Chips and Testing Procedure

Diagnostic test chips have been designed in such a way that both the fabrication and the design parameters can be extracted and controlled. Four 5 × 5 mm PCM chips with test structures covering all the parameters described in Section II were used.

They were placed in five representative locations on the wafer: in the center and in the middle of the four quadrants, labeled as $(+,+)$, $(-,+)$, $(-,-)$, and $(+,-)$. For over a year now, these locations have been kept the same in order to monitor the uniformity of parameters across the wafers and run-to-run reproducibility.

All electrical measurements were done entirely by an automated measurement system OCTOPUX in a shielded room. A custom designed low temperature test probe was implemented that allowed for loading up to four PCM chips at the same time. Upon cooling to LHe temperature, all the chips were measured sequentially. This allowed us to reduce significantly the time wasted on probe cooling down and warming up, both requiring human involvement and not yet automated.

Test algorithms have been developed for all of the diagnostic chips such that a single command could automatically measure, collect, and log data. A database system with a web-based interface easily accessible from the intranet has been developed to automate the display of results and to do trend analysis and correlation.

IV. Results

A. Josephson Junctions and On-Chip Uniformity

For unshunted junctions a four-point measurement was done on each array. The automated algorithm is centered on finding a median switching current that is defined as a current at which 50% of the junctions in the array switch. The data were fit to a parabolic function [11] to extract the critical current density and the "missing" radius dr as shown in Fig. 1.

Although at $\beta_c \sim 1$ a shunted junction is still slightly hysteretic, the switching voltage is much less than the gap voltage V_g and rather close to I_cR_s, where R_s is the shunt resistance.

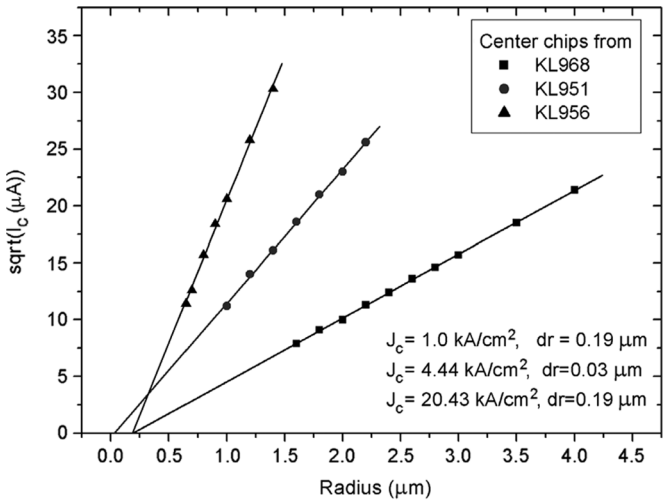

Fig. 1. Critical currents of 20-junction arrays of circular unshunted JJs of different sizes for the three current density processes. Fit to $I_c = j_c\pi(r-dr)^2$ is shown by straight lines. The data are from PCMs located at the wafer center.

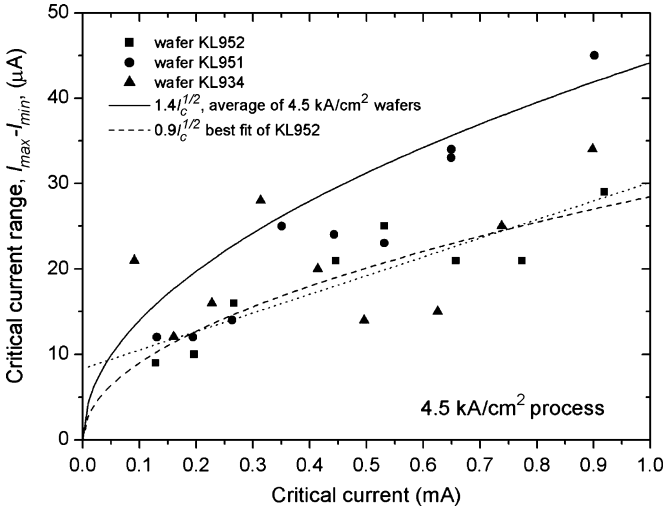

Fig. 2. The typical range of the critical current spread $I_{\max} - I_{\min}$ in 20-JJ arrays of unshunted junctions with 4.5 $\mathrm{kA/cm^2}$ critical current density. Linear fit (dotted line) and a fit to $I_{\max} - I_{\min} = kI_c^{1/2}$ are shown. Some data scattering is most likely caused by flux trapping during the automated measurements.

The test algorithm for arrays of shunted junctions was exactly the same except that the voltage level was set at 15 mV corresponding to $\sim 50 \cdot I_cR_s$ or $\sim 150\ \mu$V per junction on average.

One of the most important parameters for VLSI superconducting circuit fabrication is the on-chip uniformity of JJ critical currents. Along with defect density it determines the complexity of yieldable circuits. For all JJ sizes used in the circuits, the I_c uniformity was measured on 20-junction arrays of unshunted junctions as shown in Fig. 2. Also, 30- and 100-junction arrays were used to measure the I_c spreads for two representative values: the smallest I_c and the most frequent I_c used in the circuits. The results are summarized in Table I. The full range of spread (the difference between the largest and the smallest current in the array) was used to estimate the standard deviation σ_{I} by assuming normal distribution.

TABLE I
THE TYPICAL ON-CHIP UNIFORMITY OF THE CRITICAL CURRENT

Process (kA/cm^2)	1.0	4.5	20
Minimum JJ I_c (μA)	120	120	160
Standard deviation (μA)	4.2	3.8	6.1
Most frequent I_c (μA)	250	250	250
Standard deviation (μA)	6.1	5.5	7.6
Largest yieldable circuit size, N	$1.2{\cdot}10^4$	$2.6{\cdot}10^4$	$5.7{\cdot}10^3$

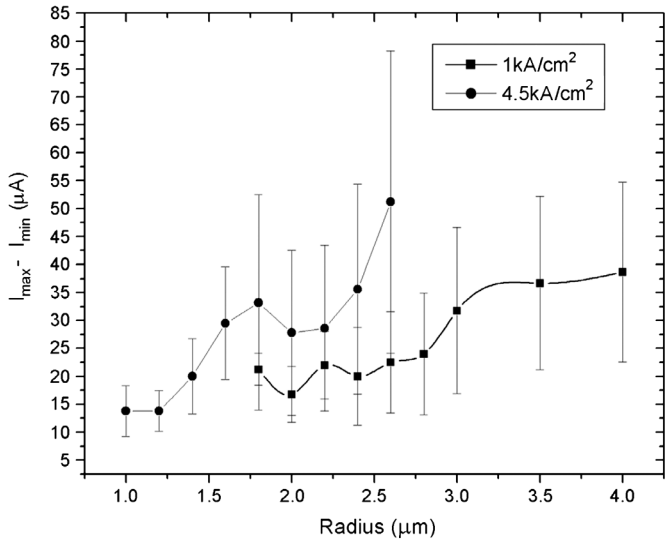

Fig. 3. Critical current variation as a function of Josephson junction radius for 1.0 and 4.5 $\mathrm{kA/cm^2}$ processes. No expected scaling with the critical current density was observed.

If we assume that the I_c spreads are mainly caused by variations of JJ dimensions induced by lithographic and etching processes, then the range of I_c variation can be estimated as

$$\delta I_c = 2\pi r \delta r j_c = (4\pi j_c I_c)^{1/2} \delta r \tag{2}$$

where δr is the range of variation of the junction radius. The fit to this $kI_c^{1/2}$ dependence is shown in Fig. 2 for one of the wafers as well as for the averaged data on 5 wafers. A linear fit, $a + bI_c$, is included for a comparison. The smallest I_c spreads were found in the 4.5 $\mathrm{kA/cm^2}$ process, though the $kI_c^{1/2}$ dependence describes the critical current spreads for other current densities as well. The average coefficient k was found to be 1.54, 1.40, and 1.92 for 1.0, 4.5 and 20 $\mathrm{kA/cm^2}$ processes, respectively. Estimating the range of JJ radius variation δr from the values of k, we find δr to be from ± 0.02 to ± 0.08 μm, that turns out to be close to the accuracy (the beam spot) of our e-beam-written, 1x projection photo-masks.

However, what we find surprising is that k is almost independent of the j_c, although, in the model of junction size fluctuations caused by lithography and etching, k is proportional to $j_c^{1/2}$ as in (1). In order to investigate this issue further, we compared the critical current variations in junctions of the same nominal radius, printed using the same photo-mask but with different current density, as shown in Fig. 3. For the junctions of a given size, one would expect the current spreads to grow with j_c. However, for small JJ sizes, the spreads in 4.5 $\mathrm{kA/cm^2}$ junctions are less than in 1 $\mathrm{kA/cm^2}$ junctions. This strongly suggests that the observed variations of I_c are not related to random variations of the junction sizes but have a different origin.

A likely candidate is variations of j_c rather than the junction size. In this model $\delta I_c = I_c(\delta j_c/j_c)$, that would correspond to term bI_c in the linear fit in Fig. 2. The measurement equipment noise could be responsible for the constant term a. The j_c variations can be caused, e.g., by a charging damage to tunnel barriers induced during plasma processing steps of the wafer fabrication. This damage mechanism should diminish as j_c increases due to increase in junction normal conductance. So, it is possible that only a part of the observed I_c spreads is intrinsic. More research is needed to clarify this issue.

The cells of HYPRES design library have I_c margin of $\pm 20\%$ with respect to a uniform shift of I_cs of all junctions or a random deviation of any single junction. However, the influence of random variations of I_cs of many junctions on complex ICs is not known. A common belief is that the critical current of any junction should not deviate from the target by more than $\pm 10\%$. That is $\mathrm{USL} - \mathrm{LSL} = 0.2I_{ci}$, where USL and LSL are the upper and lower specification limits, respectively. Statistically, this condition is most difficult to satisfy for the smallest and the most frequently used JJ in the circuit.

Assuming the normal distribution of junction I_c variation, the average maximum number of junctions in the yieldable circuit, N can be estimated as $\min\{(2f_i \cdot P(z_i, \infty))^{-1}\}$. Here $\mathrm{P}(z_i, \infty)$ is the far right tail probability of the normal distribution, f_i is frequency of appearing of the i-th junction, $z_i = 0.1I_{ci}/\sigma_{\mathrm{i}}$, and σ_{i} is the standard deviation of critical current I_{ci}. The f_i for the smallest JJ in the typical HYPRES circuit is 0.02 and for the most frequent JJ is 0.5. Then, using the data in Table I, $z_i = 2.86$ and 3.16 for 1.0 and 4.5 $\mathrm{kA/cm^2}$ processes, respectively. The estimate for the maximum yieldable circuit becomes, respectively $N \sim 1.2 \cdot 10^4$ and $2.6 \cdot 10^4$. Considering only the most frequently used JJ would give $N \sim 4.8 \cdot 10^4$ for 1.0 $\mathrm{kA/cm^2}$ and $\sim 7.4 \cdot 10^4$ for the 4.5 $\mathrm{kA/cm^2}$ process, i.e. much larger circuits. The currently observed good yield of $1.1 \cdot 10^4 -$ JJ circuits seems to support the validity of these estimates.

So we see that the maximum yieldable circuit complexity is determined by deviations of the smallest junctions in the circuits from the target value. This statistical observation is in a good agreement with experimental results on low-speed testing of digital filters where failure of the circuit could be traced to a particular logic cell and ultimately to a particular junction or a small set of junctions [16]. Therefore, further improvements in the lithography are necessary in order to achieve VLSI level of fabrication, especially for the high-j_c processes. If the cost of lithography upgrade is prohibitive, the same result can be achieved by increasing the minimum JJ size and by decreasing the frequency of its appearance. These design solutions may well be a less costly alternative to a hardware upgrade.

B. Run-to-Run Variations

Monitoring j_c in five locations on the wafer has allowed us to reveal the existence of a reproducible nonuniformity of j_c over the wafers. Most notably, the j_c in the middle of the third quadrant $(-\mathrm{x}, -\mathrm{y})$ is significantly (up to ~50%) larger than in

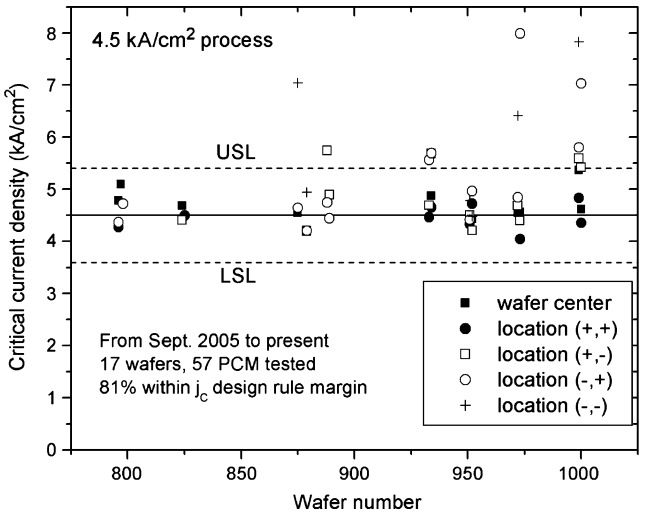

Fig. 4. Average critical current density extracted from arrays of shunted and unshunted JJs in five locations across 4.5 $\mathrm{kA/cm^2}$ wafers. The data on shunted and unshunted arrays agree within $\pm 5\%$. The target j_c is shown by a solid line, and dashed lines show the upper and lower specification limits.

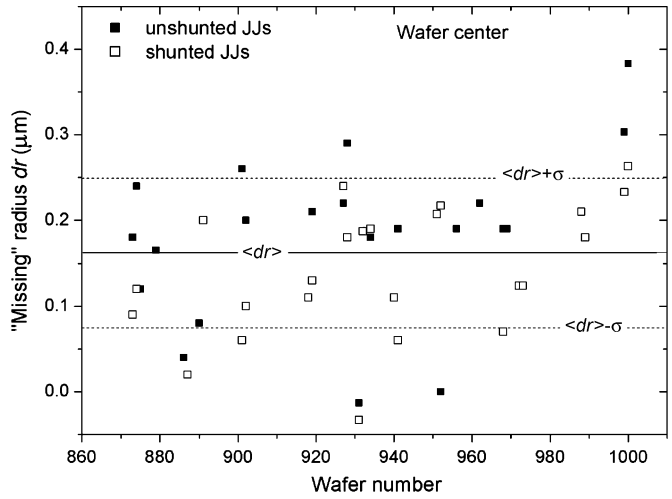

Fig. 5. Run-to-run variation of the Josephson junction size bias ("missing" radius) in the center of wafers produced since Sept. 2005 (data on 1.0, 4.5 and 20 $\mathrm{kA/cm^2}$ current density processes included). Mean $\langle dr \rangle = 0.16$ μm, $\sigma = 87$ nm.

other locations on the wafer. The possible causes of this effect are currently under investigation. If this "hot spot" is excluded from the analysis, the j_c variation over the rest of the wafer is within $\pm 10\%$.

The trend chart in Fig. 4 shows the j_c in different locations on the wafers since the 4.5 $\mathrm{kA/cm^2}$ process monitoring has been started. Without the $(-,-)$ region, the average j_c over all wafers produced in 2006 is $\langle j_c \rangle = 4.85$ $\mathrm{kA/cm^2}$ with standard deviation $\sigma = 0.736$ $\mathrm{kA/cm^2}$. The design margin on j_c for HYPRES circuits is $\pm 20\%$. That is the $\mathrm{USL} - \mathrm{LSL} = 0.4 j_c$. For the 4.5 $\mathrm{kA/cm^2}$ process, the capability index $\mathrm{C_p} = (\mathrm{USL} - \mathrm{LSL})/6\sigma = 0.41$ is less than 1, indicating that the process is still very immature from the point of view of statistical process control (SPC). However, if only a central part of the wafer or $(+,+)$ quadrant is considered, the capability index becomes acceptable, $\mathrm{C_p} = 1 - 1.2$. It indicates that the main problem that needs to be addressed is non-uniformity of the critical current across 150-mm wafers rather than run-to-run reproducibility.

One can see from above that the mean, $\langle j_c \rangle$ is higher than the target value for the 4.5 $\mathrm{kA/cm^2}$ process. From the point of view of SPC, this indicates an incorrectly centered process. However, a decision was made to introduce no corrective measures (e.g., do not change tri-layer oxidation parameters) and keep the $\langle j_c \rangle$ a bit higher than the target. An annealing at 215 °C in inert atmosphere was used to reduce the critical current density on chips of interest. This allowed us to study the operation of the very same SICs at different critical current densities in order to accumulate statistical data on margins of operation of different SICs. With this additional tool of j_c adjustment, practically any chip on the wafers could be brought to the proper j_c that made it operational.

Fig. 5 shows the run-to-run variation of the "missing" radius dr in the center of the wafers. It is interesting to note that there is small statistical difference between the dr values extracted from arrays of shunted JJs and unshunted JJs. This difference could have been expected because the critical current of small unshunted junctions could be more suppressed by noise that effectively would look like "missing" junction area. The mean "missing" radius $\langle dr \rangle$ was found to be 0.16 μm with standard deviation of $\sigma = 87$ nm. The run-to-run dr distribution was found to be very close to the normal distribution, with skewness $a_3 = -1.5 \times 10^{-3}$ and kurtosis $a_4 = 3.03$ (for purely normal distribution they are 0 and 3, respectively). In the past, compensation for $dr$was done in the individual designs. Since March of 2006, a uniform compensation has been applied to the photo-masks. Although the cells of HYPRES design library have I_c margin of $\pm 20\%$, the influence of a systematic shift of critical currents of all junctions in complex ICs is not exactly known. A deviation of dr from the target causes a systematic, nonlinear shift of all critical currents in the circuit $dI_{ci} = (4\pi j_c I_{ci})^{1/2} \cdot dr$. A common belief is that the critical current of any single junction should not deviate from the target by more than ± 20. A $\pm 20\%$ margin of I_c requires dr/r to be within $\pm 10\%$, that is dr variation of less than ± 178, ± 84, and ± 50 nm for the smallest JJs in 1.0, 4.5 and 20 $\mathrm{kA/cm^2}$ processes, respectively. With the junction size standard deviation of 87 nm determined for our process above, these dr margins correspond to $\pm 2\sigma$, $\pm 1\sigma$, and $\pm 0.57\sigma$, respectively. Even well centered on the mean, the current lithography process may likely produce, respectively, 1 out of 22, 1out of 3, and 2 out of 3 wafers out of specs on dr for 1.0, 4.5 and 20 $\mathrm{kA/cm^2}$ runs, respectively.

The junction specific capacitance was extracted from an $I-V$ curve of a small junction RF-coupled to a large junction, similarly to [14]. A pronounced step on the $I-V$ curve was observed, corresponding to the plasma resonance in the large junction $\omega_\mathrm{p} = (2\pi j_c/\Phi_0 C_s)^{1/2}$. The specific capacitance data obtained in this way for 1.0 $\mathrm{kA/cm^2}$ process are: $C_s = (55.9 \pm 3.2)$ $\mathrm{fF}/\mu\mathrm{m}^2$, averaged over 9 wafers. For the 4.5 $\mathrm{kA/cm^2}$ process, only four test structures were measured from three wafers, giving $C_s = (63.4 \pm 1.0)$ $\mathrm{fF}/\mu\mathrm{m}^2$.

TABLE II
SUMMARY OF AVERAGE INDUCTANCE MEASURMENTS

Inductor configuration	Normalized sheet inductance, L_{sq}/L_0 (L_0=2.63 pH)	Fringing factor (μm)
M0-M1	0.18 ± 0.01	0.48 ± 0.32
M0-M1-M3	0.15 ± 0.01	0.34 ± 0.12
M0-M2	0.27 ± 0.02	1.15 ± 0.1
M0-M2-M3	0.16 ± 0.01	0.31 ± 0.15
M0-M3	0.52 ± 0.03	2.52 ± 0.3

C. Inductors

A summary of the sheet inductance and fringing factor measurements is shown in Table II for the five-inductor configurations (see Section II-C). The cells of HYPRES design library are optimized in such a way that any cell can tolerate simultaneous deviation of all inductances up to ±40%, and of any single inductance up to ±40%. The minimum line-width of inductors currently implemented in HYPRES circuits is 4 μm. At this minimum line-width, the inductance was found to be the easiest of all parameters to control. Trend charts (not presented here) show that during the last two years none of the five inductor configurations deviated more than ±10% from the designed value. The same is true with respect to resistors.

V. CONCLUSION

A set of diagnostic chips has been developed for monitoring HYPRES superconducting IC fabrication process and extracting all the design parameters. It was found that the most reproducible and easiest to control parameters are inductances and resistors. The most difficult to control is the run-to-run variation of the Josephson junction size and across the 150-mm-wafer uniformity of the critical current. The observed on-chip I_c spreads cannot be explained by random variation of JJ sizes caused by lithography and etch processes. The I_c uniformity of the smallest junction in the circuits determines the size of the largest yieldable circuits. Deviations of I_c of the smallest junction from the target are the main source of circuits' failures. Although the existing 1.0 and 4.5 $\mathrm{kA/cm^2}$ processes are capable of yielding circuits with ~20 k junctions, significant upgrade of lithography is required for the 20 $\mathrm{kA/cm^2}$ process that is currently under development.

ACKNOWLEDGMENT

We are grateful to V. K. Semenov, T. V. Filippov, D. E. Kirichenko, and I. V. Vernik for many discussions, to A. Sahu, D. Amparo, and A. Talalaevskii for their help with some of the measurements, and to J. A. Vivalda, R. T. Hunt, and D. A. Donnelly for their part in the wafer processing.

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