Invited Paper

Josephson readout electronics for the hybrid superconducting pixel detector

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Abstract. We have recently demonstrated the Hybrid Superconducting Pixel Detector (HSPD) principle using a test configuration. This demonstrator device consists of a semiconductive particle detector coupled to a Josephson Tunnel Junction (JTJ) acting as current sensitive discriminator. We used Minimum Ionising Particles (MIPs) as events generators. Experimental data show the first case of MIPs detection using JTJ. The efficiency of the demonstrator circuit reaches 90% with 2 MIPs and it will be improved once the complete device will be full integrated in one circuit. A second generation demonstrator, involving an eigth channel readout scheme fully implemented with superconducting electronics is being developed and will be discussed in some detail.

1. INTRODUCTION

A new position detector using Josephson Tunnel Junction (JTJ) has been recently proposed[1]. High radiation hardness, fast switching time (t_{switch} about 1 ps) and full integration with superconductive latching logic technology (4JLs or RSFQ) are the main features of this detector.

The radiation hardness of bulk superconductors is well known. However very few studies have been done on the effect of ionizing radiation on Josephson Tunnel Junctions (JTJs) [2,3], and only recently on junctions made using state of the art Nb technology [4,5]. Lately the response of Nb-based Josephson junctions and RSFQ digital devices to a beam of 6.5 MeV protons has been investigated. A total fluency of 10^{16} p/cm^2, corresponding to a radiation dose of 5 Grad, has been reached [6,7] . The junction characterizations, both at 4.2 K and 1.2 K, show no appreciable changes due to the radiation. A deterioration effect can be seen on few large area junctions belonging to the large size array of the chip, and can be ascribed to barrier damages induced either by the impinging particles or by the thermal cycling. The digital circuits, which employ much smaller junctions, showed no changes in their operating margins. These results indicate a very interesting potential for application of superconductive devices as fast detectors and signal processors in large accelerator detectors , where semiconductive devices experience serious radiation damage problems.

The use of JTJs as fast position detector has been proposed since a long time [8]. However, in the case of high energy particle such as minimum ionising particles (MIPs), the limited sensitive area (few μm^2), implicit in the hot-spot detection mechanism [9], is a major limitation for the development of high efficiency detector circuitry. Therefore a new approach has been proposed, combining in a hybrid configuration the efficiency of semiconductive sensing elements in detecting MIPs with the radiation hardness of JTJs read-out device. As current semiconductor pixel detectors exhibit poor radiation hardness essentially in the read-out electronics [10], this approach results in a dramatic improvement of the detector performances. Moreover, radiation hard semiconductors (e.g. CVD diamond) are fully compatible with the proposed scheme, while even conventional semiconductors (e.g. Si) are expected to reveal hardness to radiation once cooled at the temperature necessary for the JTJ technology (4.2 K). Moreover, since the JTJ sampling element is current driven, several semiconductors can be considered as absorbers. In fact, where the detector generates a smaller total collected charge (e.g. due to a smaller charge collection distance), a higher drift velocity compensates this effect, leaving almost unchanged the excess current pulse amplitude.

As natural interface to the signal produced by the JTJ sampling elements, Josephson logic circuits have been considered, which conjugate a large radiation hardness and very fast signal processing speed. Since the switching time in a JTJ is of the order of few ps, it has been immediately clear the possibility to use these devices to realize logic circuitry faster than traditional semiconductive one. Moreover the low dissipation, proper of devices made by superconducting materials, allows a higher level of integration of microcircuits. At the end of the 1980s the product $P_d \cdot t_d$ (dissipating power times delay time) of Josephson logic gates ranged around 100 ps·μW, while the semiconductive ones showed their best point to be nearby

10 ps·mW, that is two orders of magnitude less [11]. Various Josephson logic families are available at present time. They differ in the definition of the binary logic levels ("1" and "0") and in the way to transmit this signal from one gate to another. The two main classes of Josephson logic families are called: 'Latching' and 'RSFQ' (Rapid Single Flux Quantum). The former uses substantially underdamped junctions exhibiting hysteretic current voltage characteristics [12]. As long as a gate is in the superconductive state his output voltage is 0 (level "0"). Once the device switches to the resistive state, an output voltage of 2.8 mV appears (level "1") and the gate itself holds this state until a reset signal (that is a reset of power bias) occurs. This last feature is the reason of the name 'latching' assigned to these circuits, and their input/output are considered "dc-signals" since the relatively long duration. The clock signal of each and every gate must be external in this case, and every logic operation takes one clock cycle. On the other hand an RSFQ device uses overdamped junction, which do not have hysteretic characteristic. In this approach the binary information is not represented by a dc-voltage, but by a very short (picoseconds) voltage pulse at gate terminals. The area of this pulse is a single flux quantum (SFQ) $\phi_0 = 2.07$ mV·ps. The essence of this idea is that SFQ can be transmitted ballistically inside a certain block of a complete circuit, and the clock signal is physically similar to the signal pulse. Therefore such a block can function without any external control signal enhancing the operation speed of the entire circuitry [13].

Several examples of full operating microprocessor have been realized in the past years. An example is the prototype named "4-bits Josephson computer ETL-JC1" realised at Electrotechnical Laboratory in Tsukuba (Japan) [14]. This design contains four Josephson LSI chips including register and arithmetic logic units, sequence controller, 1280-bit ROM unit and 1-Kbit random access memory bank, and incorporates 22000 junctions in the total circuit. The central processing unit (CPU) of this prototype is able to process 10^9 instructions per second (GIPS). Present studies focus on the performance's improvement of each logic units. Recently, for example, a new Josephson random access memory banks has been presented [15]. This RAM is made by 21000 Josephson junctions and can process 4-Kbit with a access time of 380ps: the fastest of any memory chip reported. Nowadays the lithography of circuits is the main limitation to enhancing speed and enlarging parameter range, therefore circuitry progresses go along with fabrication technologies. For this purpose, electron beam direct writing technique can be used to pattern directly on the wafer the smallest parts of a circuit [16]. A small scale logic integrated chip, containing 100 basic gates, has successfully showed a delay time of 8.6 ps/gate. Recently a new film deposition process for high quality circuits has been achieved by using Electron Cyclotron Resonance [17]. This improvement will set a new J_c spread estimated at about 0.1% on the entire chip.

2. RESULTS ON A SINGLE JUNCTION

An experiment to demonstrate the effective sensitivity of a JTJ in detecting MIPs when connected to a semiconductive detector has been recently carried out [18]. The HSPD demonstrator is realized by connecting a silicon detector (either a p-i-n diode or an ohmic contact device) to a JTJ which acts as current sensitive discriminator. In Fig. 1 is shown a schematic representation of this device, together with its equivalent circuit.

The test structure was assembled using two separate chips (detector and JTJ discriminators) wire bonded to implement the HSPD configuration. This is certainly non ideal, because of the effect of stray inductances, nevertheless it is a suitable choice for a first test.

The JTJs used were high quality Nb/AlOx/Nb junctions fabricated both at Electrotechnical Laboratories (Japan) and CNR Istituto di Cibernetica (Italy). The dimensions ranged from 3x3 to 10x10 μm^2 leading to different critical currents. Fine tuning of the junction critical current was also possible by applying an external magnetic field. The silicon detectors were 3x3 mm^2 in dimensions and 420 μm in thickness processed at Brookhaven National Laboratory out of n-type 5-8 kΩ-cm Silicon. The ohmic devices were obtained using implanted layers leading to a Al/n+/n/n+/Al structure.

The measurements were made using a 1 mCi Ru^{106} beta source (active area 5 mm in diameter) collimated through a 3 mm hole in a 1mm thick lead foil placed just in front of the detector. The distance between the source and the detector was 2.6 mm. To allow a proper cooling the experimental chamber was immersed in liquid He (T=4.2K) and filled with 10 mBar He exchange gas.

The Si chip acting as detector, can be represented by an ideal current generator due to its very high internal resistivity, peculiar to Si at very low temperature (4.2K). Such a system, once properly biased, realises a Si detector with non-blocking electrodes, coupled to a current sensitive sample and hold JTJ element. At such a low temperature, the saturated electron drift velocity is achieved for a drastically reduced voltage [19]. Besides, the contribution of holes rises up, their velocity becoming only one half of that of the electrons [20]. This leads to a non negligible contribution of the holes to the total signal that give us the time dependence of the collected charge.

The junction is biased in the zero voltage state, with $I^*_{bias}<I_c$. Applying a voltage V_{HV} to the electrodes of Si chip, the total current flowing in the junction will be the sum of the bias current and the Si leakage one (I_{leak}): $I_{bias}=I^*_{bias}+I_{leak}$.

Assuming that the bias point is far from the noise activation threshold, the junction will indefinitely persist in the zero voltage state until an excess current pulse (due to a MIP passage) brings the overall current flowing in the junction above the critical value. Then, in a time of the order of 1 ps, a switching to the junction the gap voltage (2.8 mV) occurs. This state remains stable until the current bias is removed (AC bias). Typical values for excess current pulse amplitude result to be in the order of 2-4 μA [19].

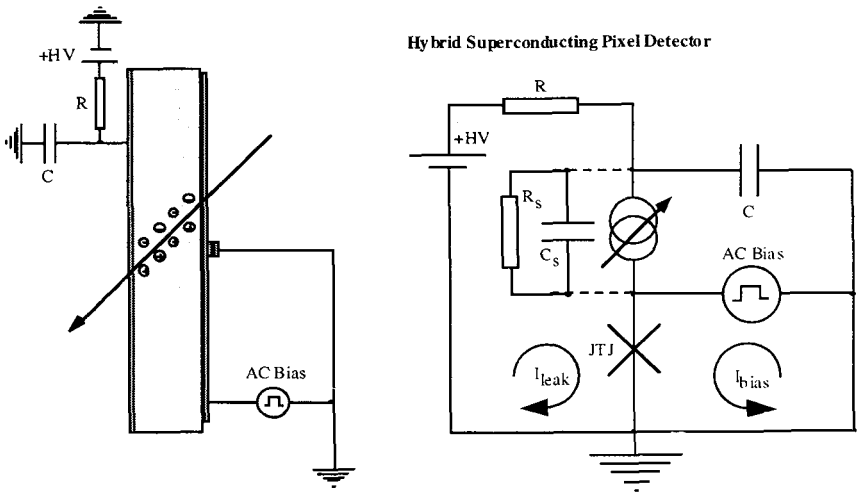

Figure 1: (left) Schematic representation of the tested demonstrator HSPD. (right) Equivalent circuit.

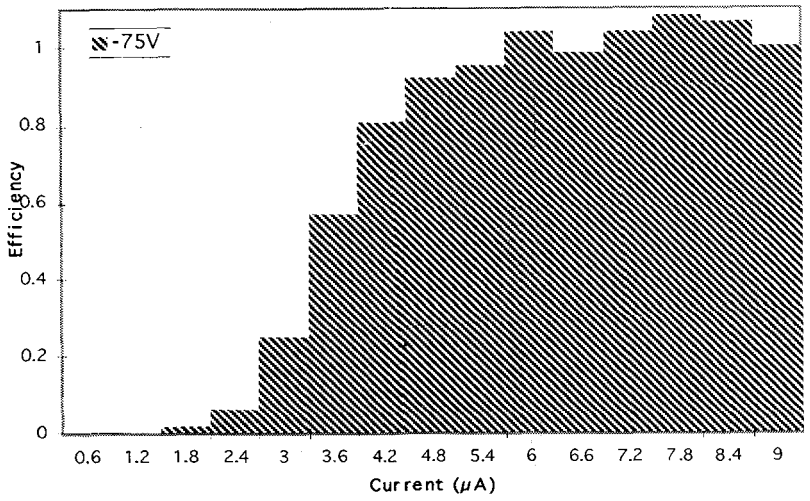

Figure 2. Trigger efficiency of the tested demonstrator HSPD vs signal current amplitude from the silicon detector.

The experimental configuration includes also a charge amplifier connected to the silicon detector, providing a signal with amplitude proportional to the number of charges generated in the silicon, and therefore to the energy of the impinging particle. For the charge measurements a shaping time of 2 μs was used .

In order to measure the efficiency of our JTJ discriminator to detect current pulses produced by the silicon detectors, first the spectrum of the Ru^{106} source was recorded for a certain time, with the junction unbiased. Afterwards, keeping exactly the same bias parameters for the detector, the JTJ was biased using the synchronous clock. In this way it was possible to observe coincidences between JTJ switch and signals in the detector. The JTJ switch signal was used to trigger the pulses acquisition, in order to build a spectrum containing only particles that caused a switch of the JTJ. The ratio between the spectra acquired in these two ways gives the efficiency of the detector. However, as the HSPD is a current sensitive detector, to obtain the efficiency in detecting particles, the previous results should be translated from charge to current. We refer to the comprehensive work of ref. [19] that investigated the pulse shape of signals produced in Si detectors down to 8 K, this allows the computation of the peak current amplitude from the total collected charge. By using a simple constant field model for the ohmic device, in which the field is strong enough to saturate the carrier drift velocity, and taking into account the capacitance of the detector we concluded that a MIP. produces a current signal which amplitude is 2.4 ± 0.1 μA for the ohmic device.

In Fig. 2 is shown the efficiency plot obtained for the ohmic detector. The ohmic device showed 90% efficiency for signals of 4.8 μA or 2 MIPs In the case of the diode, due to the larger capacitance, the previous values were 5 μA and 2.5 MIPs respectively.

Of course, in order to scale the proposed scheme to a few thousand channels detector a major improvement in term of sensitivity is still needed.

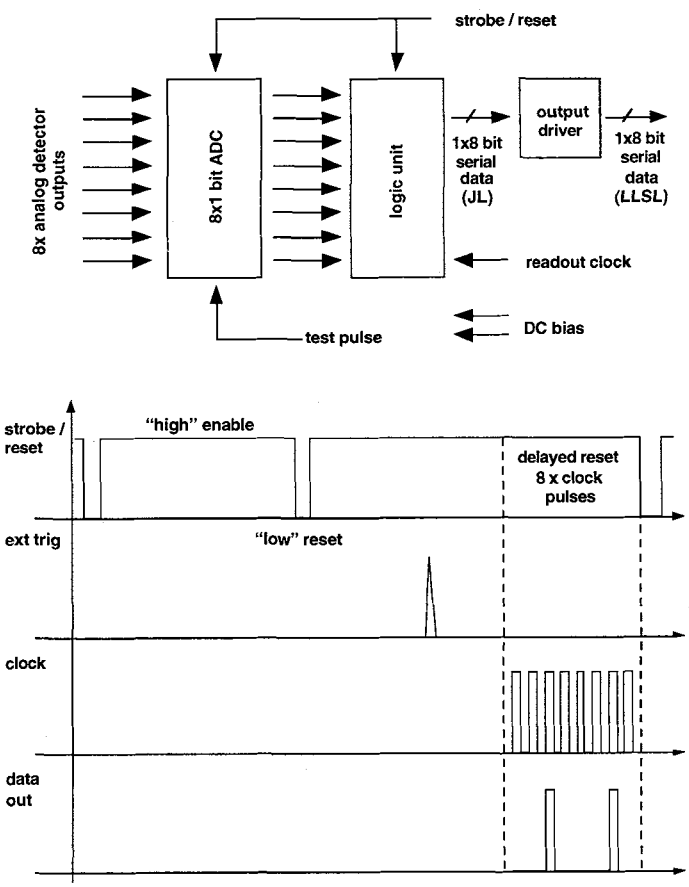

Figure 3. Block diagram of an 8-bit detector readout chip based on RSFQ circuitry.

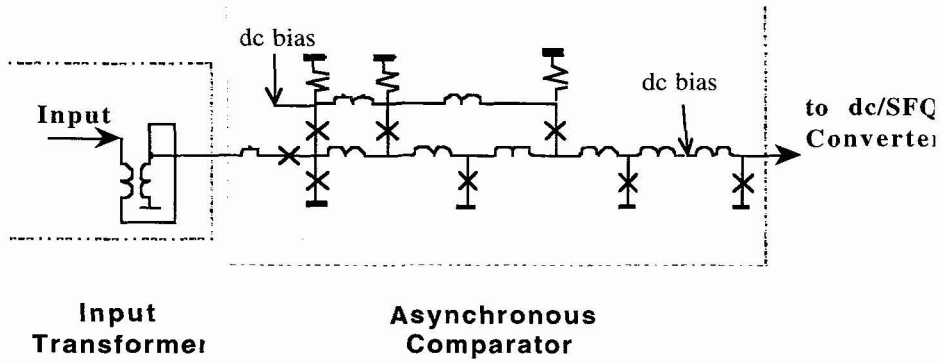

Figure 4. Schematic of the front-end section of the ADC-gate.

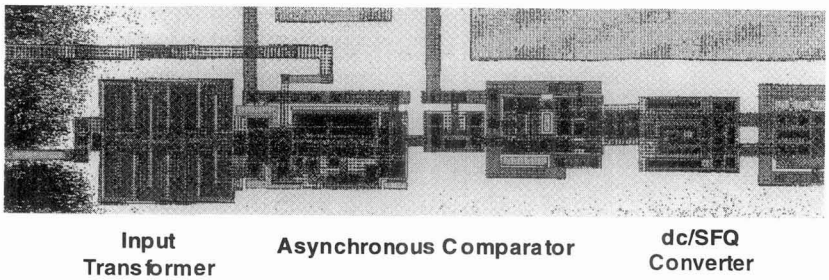

Figure 5. Layout of the ADC-gate, occupying an area of 540 μm x 90 μm.

3. READOUT CIRCUITS FOR HSPD

The next step in the direction of a multichannel detector is the integration of few pixel detectors with a common superconducting readout electronics. In fig. 3 is shown the block diagram of an 8-bit detector which is being developed. The circuit operation is also shown in the figure, and can be summarized as follows.

A strobe/reset signal periodically resets all the readout logic to a known state, will all zeros in the detector lines. When an external trigger signals the passage of a mip through the detector, the reset is hold inactive (high) and a series of clock pulses is sent to the logic unit. This unit acts as a shift register on the data collected by the ADC converters, and sends the serialized data to the output driver. Here the low level Josephson logic signals are converted to voltage pulses with amplitude sufficient (10mV) to drive a semiconductive logic.

Although the superconductive circuit is capable of working with clock frequencies in excess of 1 GHz, the first tests will be performed at much lower frequency, in order to maintain compatibility with the existing data acquisition systems.

We have been developing readout RSFQ circuitry to sense weak signals (1 μA/8 ns - 8 μA/1 ns) generated by a separate detector chip and convert them to digital signals. Each channel of the readout circuit consists of an Analog-to-Digital Converter gate (ADC-gate), a logic unit, and an output driver (Fig. 3). The 8-channel ADC-gate array senses eight input signals generated by the detector chip, then converts the weak input pulses into a single-flux quantum (SFQ) form. The RSFQ logic unit latches and performs a serial-to-parallel conversion of these eight SFQ pulses, creating a digital 1 x 8 bit serial data stream. Finally, an output driver amplifies and converts the output digital SFQ data into an 8-10 mV output voltage pulse, which is then available for the external electronics.

The design of this readout circuit is based on the HYPRES analog-to-digital and digital RSFQ technology. It takes advantage of HYPRES' RSFQ dual-ground plane logic gate library. The design of the ADC gate is based on the use of an RSFQ asynchronous comparator with input transformer and dc/SFQ converter. The comparator resolves and amplifies the weak input signal to a level sufficient to produce an SFQ pulse with our standard dc/SFQ converter. The generated SFQ pulse is delivered to the RSFQ Logic

Unit via a Josephson Transmission Line (JTL) stages. Fig. 4 shows a schematic of the RSFQ asynchronous comparator with input transformer. Fig. 5 shows a complete layout of the ADC-gate.

The RSFQ Logic Unit is a combination of standard RSFQ latches and a serial-to-parallel converter. The latches are integrated into shift register using RSFQ confluence buffers to form the serial-to-parallel converter. The SFQ pulses are captured in the latches and serially read-out by external low-speed (kHz) clock.

The design of the output amplifier is based on HYPRES' dc-driven output voltage driver. It consists of a low-voltage, low output impedance SFQ/dc converter, a Josephson transmission line (JTL) current amplifier, and a stack of dc SQUIDs.

4. CONCLUSIONS

The MIP detection capability of a HSPD cryogenic detector based on superconducting electronics at 4.2 K has recently been demonstrated. The tested HSPD scheme uses a single Josephson junction as current sensitive discriminator. However for a practical tracking detector with thousand of channels the performances obtained so far are not sufficient. A substantial improvement of the sensitivity of the HSPD by using a superconducting transformer is being tested, together with the monolithic integration of digital JTJ electronics on the detector chip.

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