High-Speed Interchip Data Transmission Technology for Superconducting Multi-Chip Modules

Deepnarayan Gupta, Wenquan Li, Steven B. Kaplan, and Igor V. Vernik

Abstract— **We have developed an interchip data transmission scheme through passive transmission lines on a multi-chip-module (MCM) carrier and 100-μm solder bump bonds. In rapid single flux quantum (RSFQ) logic, digital data are in the form of single flux quantum (SFQ) pulses. A reliable scheme for transmission of SFQ pulses through non-superconducting solder bumps between chips through a passive MCM substrate is yet to be established. Therefore, we have devised a scheme that converts SFQ pulses into toggles in a voltage waveform for interchip transmission. Data in the form of SFQ pulses are reconstructed from this voltage waveform using a sensitive quantizing pulse receiver. Our objective is to eliminate the need for amplification of the transmitted signal. This is achieved by increasing the receiver sensitivity. However, a sensitive receiver, a dc SQUID, may produce more than one SFQ pulse for each rising/falling edge of the voltage waveform. A simple circuit, pulse resurrection logic (PRL), is employed to discard any extra SFQ pulses. Together with the sensitive quantizer, the PRL circuit makes our scheme error tolerant. We have demonstrated the receiver operation using 3-μm Nb RSFQ circuits at frequencies up to 20 GHz.**

Index Terms—**Multichip Modules, Broadband Communication, Superconducting Devices, RSFQ**

I. Introduction

SUPERCONDUCTING digital electronics has always been a promising, ultra-high performance technology. The recent advances in both speed and complexity of superconducting electronics have demonstrated that this technology is now mature enough for system insertion in near future. Although most of the circuit demonstrations so far have been single chips, it is clear that future commercially viable systems will consist of multiple chips. Therefore, it is essential to develop the required infrastructure to allow integration of multiple superconducting ICs for the next generation of digital superconducting electronics.

In a multi-chip module (MCM), clock and data signals must sustain the on-chip transmission speed between chips. In RSFQ logic, digital data are in the form of single flux quantum pulses. Interchip transmission of SFQ pulses has been demonstrated using an active transmission line at low (<500 Hz) speed with good operating margins [1]. Other approaches include either synchronous [2] or asynchronous [3] transmission by converting SFQ pulses to voltage levels before and recovering SFQ pulses after transmission through a passive microstrip line on the MCM carrier. So far, these passive approaches have used amplifiers – latching junctions [4], SQUID stacks [2], [3], etc. – in the transmitters, which limit the transmission bandwidth to 5-8 Gbps.

To circumvent this bandwidth limitation, in our approach, high-speed digital manipulation of low-level signals on the receiving end is performed rather than high-speed analog amplification on the transmitting end. This approach better exploits the capabilities of RSFQ digital electronics and should provide the same scaling of transmitted data rates as the speed of on-chip digital circuits with scaling of lithography. Moreover, for an MCM with a large number of chip-to-chip interconnects, a multi-layer normal metal MCM carrier may be required, where the active carrier approach will not work.

II. Principle of Operation

Our chip-to-chip data transmission approach consists of the following steps:

(1) Encode each SFQ pulse as a transition (toggle) between a high ('1') and a low ('0') voltage state,
(2) Transmit this voltage output through non-superconducting solder bumps to the MCM carrier,
(3) Use a microstrip transmission line on the carrier to transport the signal to the other chip,
(4) Generate one or more SFQ pulses on the destination chip for each toggle,
(5) Use digital logic, called pulse resurrection logic (PRL), to reject all but the first SFQ pulse.

The data transfer scheme is shown in Fig. 1. Each SFQ pulse is converted to a voltage transition for transmission through solder bumps, then converted back to an SFQ pulse by the quantizing pulse receiver (QPR) on the destination chip. Pulse resurrection logic, using a sensitive quantizer, RS flip-flop (RSFF) with true and complementary output, and confluence buffer (CB), is a simple digital error correction scheme. It allows multiple pulses to be produced for each voltage transition by the sensitive quantizer and rejects all the pulses after reproducing the first pulse at the output.

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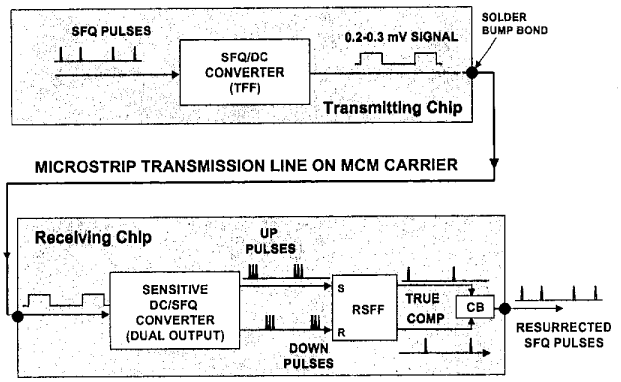

Fig. 1. The technique for transmitting data between chips in an MCM, using a transmitter to convert SFQ pulses into voltage waveforms and a receiver to convert them back to SFQ pulses.

The quantizer produces two streams of SFQ pulses (*up* and *down*) on the rising and the falling edges of the input voltage waveform. The *up* and *down* pulses are applied to the *set* and *reset* inputs of an RSFF. The first *up* pulse sets the RSFF into the "1" state, while producing a pulse at the *true* output. Subsequent *up* pulses, in the same bunch, do not alter the state of the RSFF and do not produce any output. Similarly, the first down pulse resets the RSFF to the "0" state and produces a *comp* output, while the rest are rejected. This ensures that only the first pulse of any bunch propagates through and the other pulses in the same bunch are discarded. The true and comp outputs are combined using a confluence buffer (CB) to reproduce the original data.

III. Experimental Results

The operation of the above data transfer scheme has been demonstrated by placing the transmitter and the receiver circuits on a single 5 mm × 5 mm chip, which is mounted on a 1 cm × 1 cm substrate (MCM carrier). Solder bumps are used to provide electrical connection between the two chips. All chips were fabricated at the HYPRES 3-μm Nb foundry. The flip-chip mounting was performed at TRW using 100 μm diameter InSn solder bump bonds, which are not superconducting at 4 K [5].

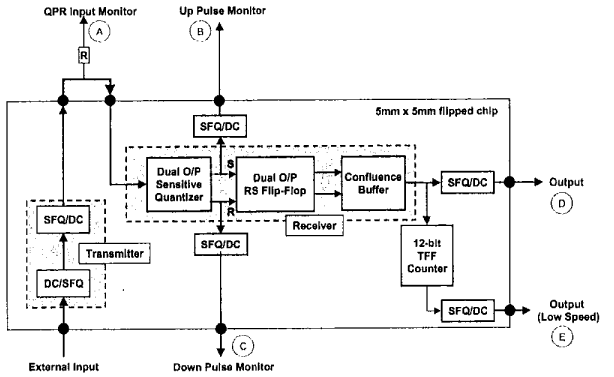

Fig. 2. Test circuit of the MCM data transfer scheme. The transmitter and receiver circuits are on a 5 mm × 5 mm chip. The solder bump bonds, between this chip and a 1 cm × 1 cm MCM carrier are shown as black circles on the circumference of this chip. All inputs and outputs are through contact pads on the substrate chip.

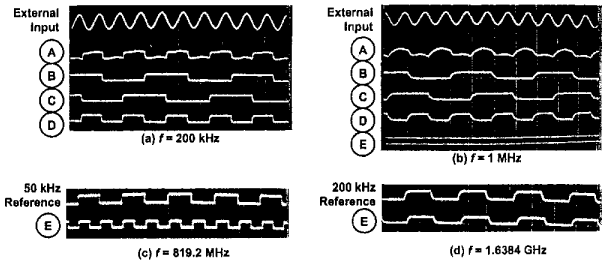

Fig. 3. The waveforms of various outputs and monitors from the MCM test circuit of Fig. 2 at different external input frequencies (*f*). At frequencies higher than a few MHz, the direct output "D" cannot be observed on the oscilloscope and only the decimated output "E" can be monitored. To verify correct frequency division ratio (2^{13} or 8192), we also display a low-frequency square-wave reference signal from an external generator.

The MCM data transfer test circuit is shown in Fig. 2. The critical component of this circuit is the quantizing pulse receiver (QPR) that converts the transitions of the transmitted voltage waveform into SFQ pulses.

Fig. 3 shows the waveforms of the up and down pulse monitors along with the receiver output at various frequencies for this test circuit. The decimated output (E), obtained by adding a chain of 12 toggle flip-flops (TFFs), facilitates monitoring the output on a low-bandwidth, high-sensitivity oscilloscope, for data transfer rates greater than a few MHz. For this chip, the waveform on the MCM transmission line (A) looks severely distorted even at low frequencies (200 kHz and higher). This is a problem of impedance mismatch at the transmission line termination. However, the quantizing pulse receiver cleans up the signal, since it does not need sharp transitions at the rising/falling edges of the waveform. This error tolerance is a major advantage of our scheme.

The apparent rounding of waveform edges (B, C, D, E) is caused due to the bandwidth limit of the oscilloscope, which acts as a low pass filter. This is evident in Fig. 3 (c) and (d), where we have displayed a square-wave reference signal of frequency equal to *f*/8192 to verify correct on-chip decimation ratio. The external square-wave signal has the same edge-rounding as the chip output.

We could test this MCM circuit only up to 1 GHz frequency due to probe limitations. However, we successfully tested the receiver itself at high frequencies (up to 20 GHz) in our 5-mm high-speed probe.

The quantizing pulse receiver (QPR) circuit layout is shown along with its functional block diagram in Fig. 4. The sensitive DC/SFQ converter is a SQUID (Superconducting Quantum Interference Device) coupled to the input through a transformer. The input signal couples flux into the SQUID and drives the SQUID across lobes in its threshold characteristic, producing an SFQ pulse as it crosses each boundary. The SQUID launches two streams of SFQ pulses – one on the rising and one on the falling edge of the input respectively – into Josephson transmission lines. Again, counters are included to allow the output waveforms to be displayed on a low-bandwidth oscilloscope for high input frequencies.

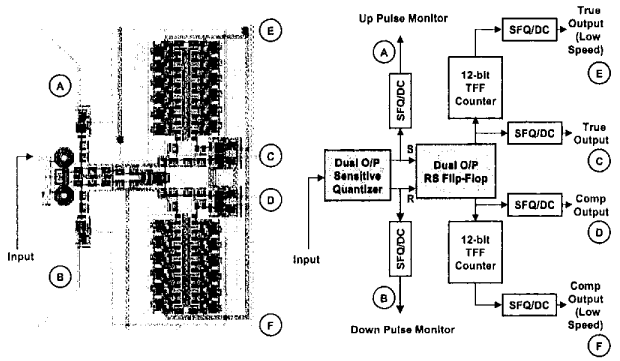

Fig. 4. The layout (left) and the functional block diagram (right) of the QPR test circuit, used as the receiver for MCM data transfer.

Fig. 5 (a) and (b) show the combined operation of the sensitive quantizer and the PRL circuits at low frequency (10 kHz), at two different input amplitudes. The quantizer is driven across a number of thresholds when the input current is applied, producing a burst of SFQ pulses corresponding to the number of thresholds crossed. The pulses produced at the rising and the falling edges of the input, referred to as *up* ("A") and *down* ("B") pulses respectively, are monitored through toggle-flip-flop SFQ/DC converters. The true ("C") and comp output ("D") monitors show the operation of the dual-output RSFF, which allows the first SFQ pulse in each bunch to propagate, while blocking the rest. This circuit showed correct experimental operation over a wide range of input frequencies. The decimated *true* (E) and *comp* (F) outputs, derived using 12-bit toggle flip-flop counters, for six different input frequencies, are shown in Fig. 6. The low-bandwidth oscilloscope acts as a low pass filter, diminishing the output amplitude and distorting its shape.

The threshold curve of the quantizer SQUID was measured. The input current sensitivity ($\Delta I_{in} = I_{n+1} - I_n$), where I_n is the minimum input current to cross the n^{th} SQUID threshold, was measured to be 32 μA. This agrees well with the theoretical value of 30.65 μA, obtained through circuit simulations. Another quantizer with ΔI_{in} = 21 μA has also been designed by changing the value of a shunt inductor across the SQUID.

To verify transmission of broadband signals through solder bump bonds, identical test circuits comprising a DC/SFQ converter, 12-bit TFF binary frequency divider, and a TFF SFQ/DC converter were placed on a 1 cm × 1 cm carrier chip as well as on a 5 mm × 5 mm chip flip-chip mounted on it. The inputs and outputs of the latter pass through solder bumps while those of the former do not.

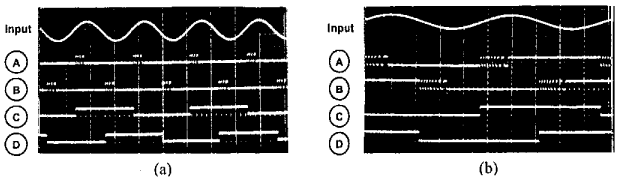

Fig. 5. Correct operation of the sensitive quantizer and the PRL circuit (Fig. 4). The quantizer produces two bunched streams of SFQ pulses on the rising and falling edges of the sinusoidal input signal respectively. All outputs are measured via toggle flip-flops; therefore, each voltage transition in the waveforms corresponds to an SFQ pulse.

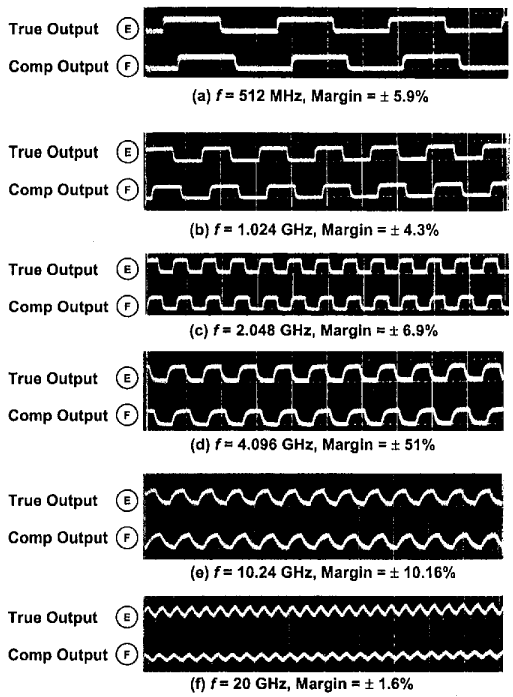

Fig. 6. The operation of the quantizing pulse receiver (Fig. 4) at different input frequencies, ranging from 0.5 to 20 GHz. The dc bias margin for the dual-output RSFF cell is indicated at each frequency. The bias margins of other circuit components were wider and these biases were kept constant at all frequencies.

An external sinusoidal clock signal was applied to these test circuits and their decimated clock outputs were monitored. The two test circuits performed with identical operating margins (±35%) up to a clock frequency (f_{clk}) of 20 GHz. Fig. 7 shows the decimated clock output waveform of the flip-chip test circuit along with an external reference square wave of the expected frequency (f_{clk}/8192).

IV. Discussion

The high-speed superconducting MCM data transmission technology using a passive microstrip line on the carrier and a sensitive quantizing pulse receiver (QPR) will provide a robust foundation for commercial, defense, and scientific products ranging from digital communications systems to high-performance phased-array radars to picosecond transient digitizers.

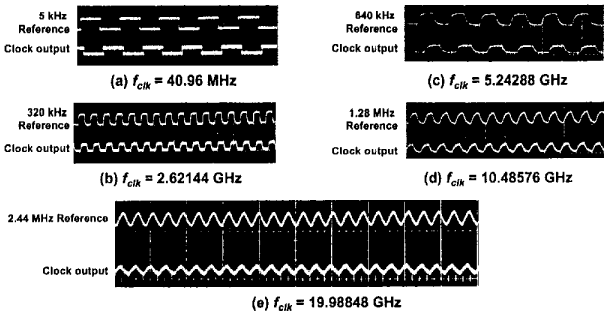

Fig. 7. The decimated clock output of a test circuit verifying the broadband transmission capability of solder bump bonds at various input clock frequencies. To verify correct frequency division ratio (2^{13} or 8192), a square-wave reference signal from an external generator is also shown.

There is a need to synchronize different blocks of circuitry, as well as to interface with other chips in a multi-chip module (MCM), which rely on SFQ-based data processing. Generation and reliable distribution of high frequency clock signals with minimal jitter and phase noise is essential in order to maintain proper gate function and to achieve peak system performance. Fig. 8 shows the combined layouts of a flipped chip and a passive carrier, designed to test interchip transmission of clock signals from a long Josephson junction (LJJ) oscillator [6]. The chip and the carrier have matching signal and ground pad configuration.

For example, a high-performance direct digital communications receiver, comprising high-resolution analog-to-digital converters, digital mixers, filters, and other digital signal processing circuitry, will enable the implementation of of a true software defined radio architecture [7]. These multi-chip systems will require fast interchip communication of both synchronous and asynchronous signals. The superconducting processing elements (SPELLs), required to build a petaflops computer processor, will consist of several processor, memory, and network switch chips in an MCM [8]. The massive clock and data distribution network required for these multi-chip modules will necessitate the use of multi-layer Cu/ceramic carrier. Only passive transmission lines can be used on non-superconducting MCM carriers. The additional loss of signal amplitude due to normal metal transmission lines is likely to be small and may be compensated by adjusting the sensitivity of the receiver.

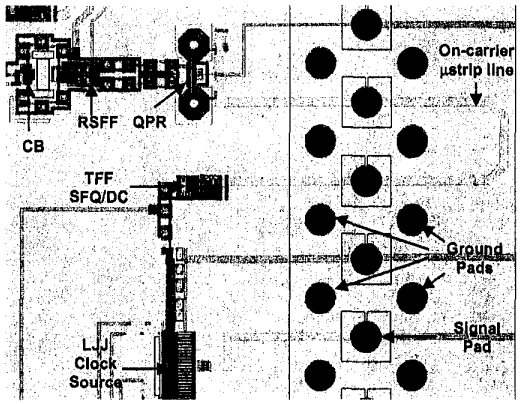

Fig. 8. The layouts of a flipped chip and an MCM carrier are superimposed at their signal and ground pads that are connected through solder bumps. The output of an on-chip clock source is transmitted through a solder bump on to a on-carrier microstrip line back to an on-chip receiver through another solder bump.

V. Conclusion

A broadband chip-to-chip data transmission technology, using passive on-carrier transmission lines and a sensitive quantizer followed by digital logic circuits, has been developed for RSFQ MCMs. Together with the sensitive quantizer, the pulse resurrection logic circuit makes this scheme error tolerant. The absence of amplifiers at the transmitter in our scheme removes additional bandwidth limitations imposed by amplifiers. This scheme has been demonstrated up to 20 GHz and is scalable as the device frequency increases with advances in junction fabrication technology. This approach should have extensive applications to complex superconducting systems such as digital radio, supercomputing, and network switches, that will require high-speed communication among multiple RSFQ chips.

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References

[1] M. Maezawa, H. Yamamori, and A. Shoji, "Chip-to-chip communication using a single flux quantum pulse," *IEEE Trans. on Appl. Supercond.*, vol. 10, pp. 1603-1605, June 2000.

[2] A. H. Miklich, A. H. Worsham, D. L. Miller, and J. X. Przybysz, "Circuits for chip-to-chip transportation of bits from single flux quantum circuits," *IEEE Trans. Appl. Supercond.* vol. 7, pp. 2278-2281, June 1997.

[3] O. A. Mukhanov, S. V. Rylov, D. V. Gaidarenko, N. B. Dubash, and V. V. Borzenets, "Josephson output interfaces for RSFQ circuits," *IEEE Trans. on Appl. Supercond.*, vol. 7, pp. 2826-2831, June 1997.

[4] J. X. Przybysz, D. L. Miller, S. S. Martinet, J. Kang, A. H. Horsham, and M. L. Farich, "Interface circuits for chip-to-chip data transfer at GHz rates," *IEEE Trans. Appl. Supercond.* vol. 7, pp 2657-2660, June 1997.

[5] R. D. Sandell, G. Akerling, and A. D. Smith, "Multi-chip Packaging for high speed superconducting circuits", *IEEE Trans. on Applied Superconductivity*, vol. 5, pp. 3160-3163, June 1995.

[6] D. Gupta and Y. Zhang, "On-chip clock technology for ultrafast digital superconducting electronics," *Appl. Phys. Lett.*, vol. 76, pp. 3819-3821, June 2000.

[7] E. B. Wikborg, V. K. Semenov, and K. K. Likharev, "RSFQ front-end for a software radio receiver" *IEEE Trans. Appl. Supercond.* vol. 9, pp. 3615-3618, June 1999.

[8] M. Dorojevets, P. Bunyk, D. Zinoviev, and K. Likharev, "COOL-0: Design of an RSFQ subsystem for petaflops computing," *IEEE Trans. Appl. Supercond.* vol. 9, pp. 3606-3614, June 1999.